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SEMICONDUCTOR DIGEST

NEWS AND INDUSTRY TRENDS

SUPPLEMENT TO JANUARY 2026

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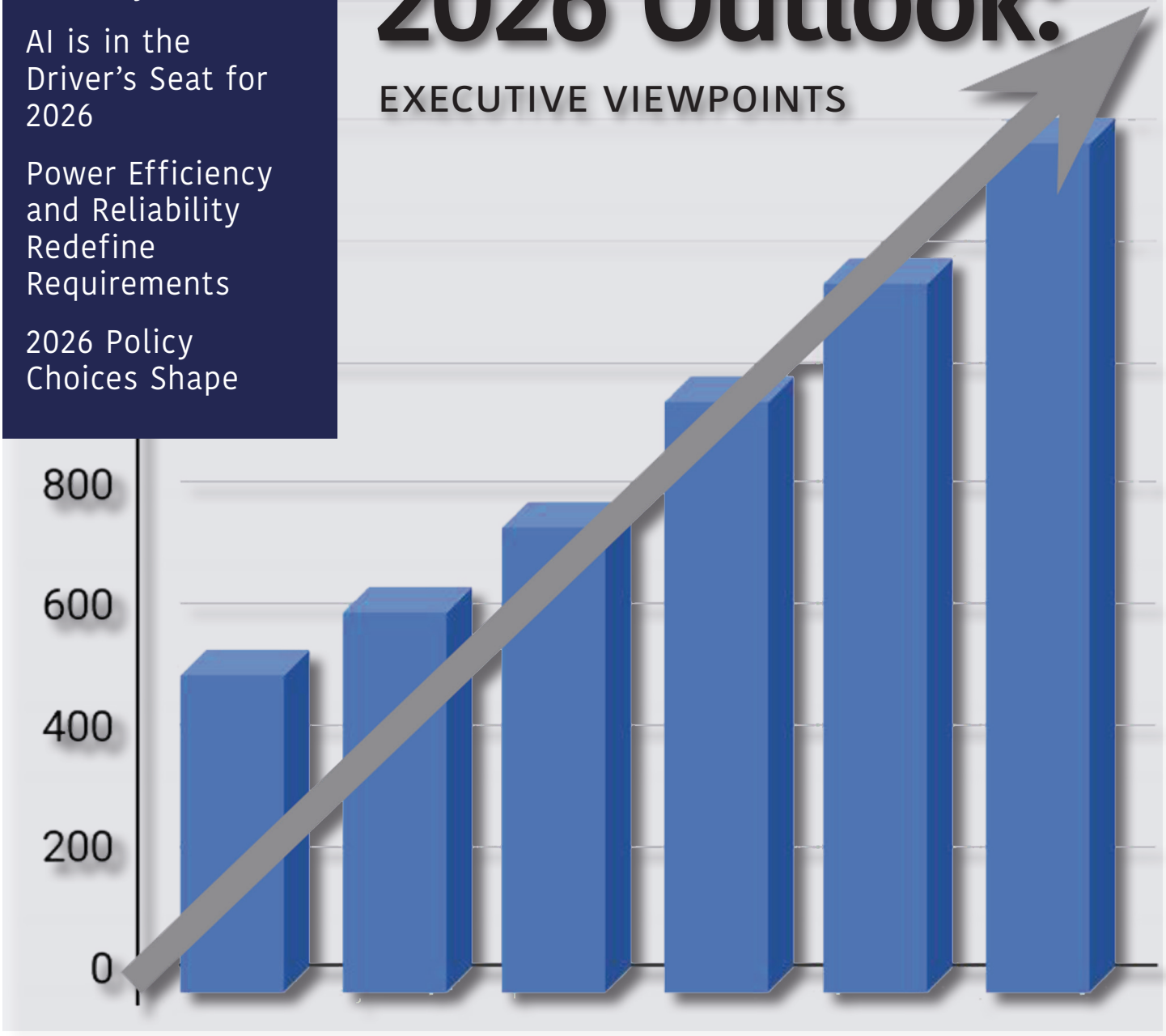

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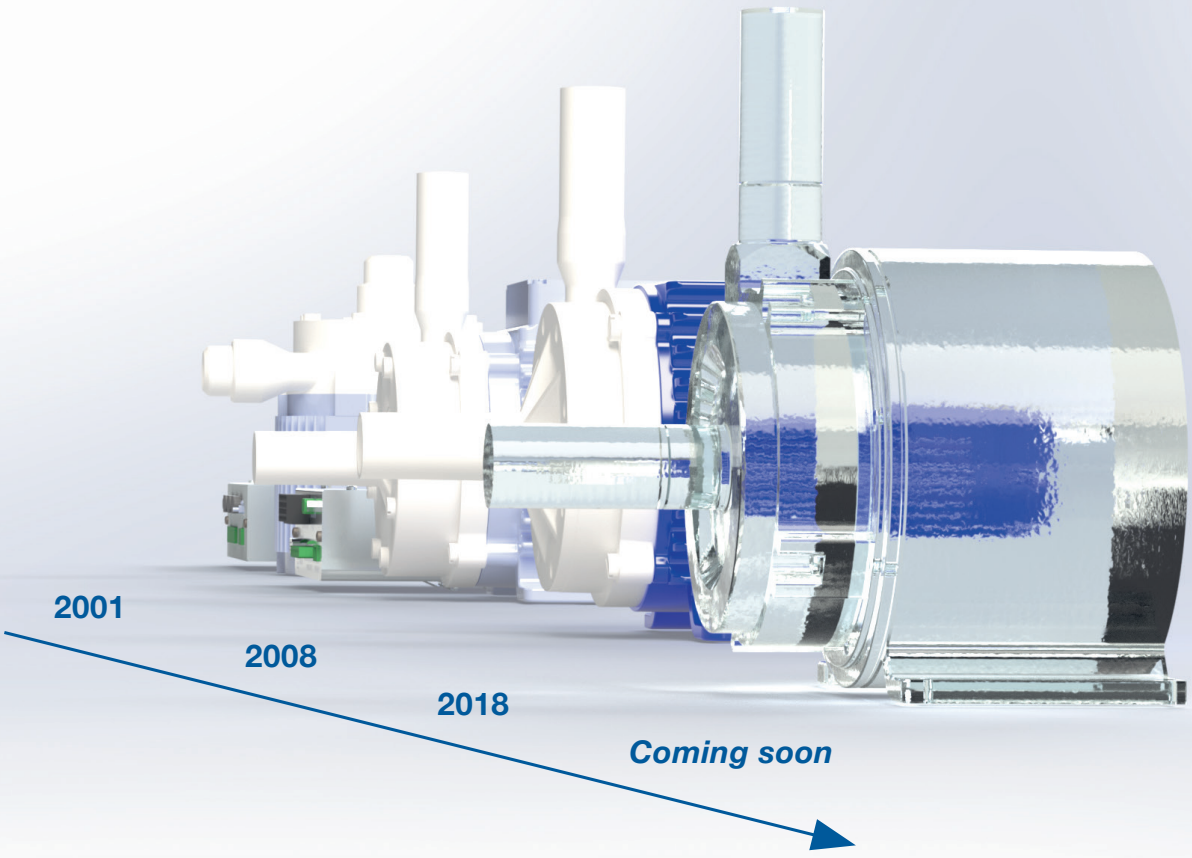

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Editorial

Here's to 2026!

THE SEMICONDUCTOR INDUSTRY'S GROWTH IS MAINTAINING ITS upward trajectory. The expectation is that it will hit the $1 trillion mark sooner than expected (as illustrated by our cover). The World Semiconductor Trade Statistics (WSTS) organization predicts that the global semiconductor market will reach $975 billion in 2026. Growth is expected across all regions and product categories. Memory and Logic are again projected to lead, both increasing by over 30 percent year over year. Most other product categories are expected to continue their gradual recovery, expanding at a more moderate pace.

Regionally, all major markets are expected to expand. The Americas and Asia Pacific remain the strongest contributors, while Europe and Japan are forecast to see low double-digit growth.

This means we are likely to hit the $1 trillion mark well before the earlier projected date of 2030.

After a record high of $133 billion in 2025, SEMI expects global sales of total semiconductor manufacturing equipment by original equipment manufacturers (OEMs) to reach $145 billion in 2026 and $156 billion in 2027. This growth will be driven primarily by investments related to AI, particularly in leading-edge logic, memory, and the adoption of advanced packaging technologies.

"Global semiconductor equipment sales show robust momentum, with both the front-end and back-end segments projected to see three consecutive years of growth, culminating in total sales surpassing $150 billion for the first time in 2027," said Ajit Manocha, SEMI president and CEO. "Investments to support AI demand have been stronger than anticipated since our midyear forecast, leading us to boost the outlook for all segments.

Rising demand from cutting-edge applications like AI, 5/6G communications, autonomous vehicles, and more has prompted industry to significantly increase global production capacity. SEMI's 300mm Fab Outlook report shows global front-end semiconductor suppliers are accelerating expansion efforts to support the surging demand for generative AI applications. The global semiconductor manufacturing industry is expected to maintain strong momentum, with capacity projected to grow at a compound annual growth rate (CAGR) of 7% from the end of 2024 through 2028, reaching a record high of 11.1 million wafers per month (wpm).

A key driver of this growth is the continued expansion of advanced process capacity (7nm and below), which is expected to increase by approximately 69% – from 850,000 wpm in 2024 to a historic high of 1.4 million wpm in 2028 – representing a CAGR of around 14%, double the industry average.

With this unprecedented growth come not only new challenges in technology, but also in fab construction, data analytics, regulations, sustainability and workforce development. Here at *Semiconductor Digest,* we seek to provide clarity on business and technical issues through a mix of news, feature articles, newsletters, on-line webinars and live show coverage. Check out our 2026 Media Planner to see how we can best work together. I'm looking forward to a great 2026!

—Pete Singer, Editor-in-Chief

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2026 Outlook: Executive Viewpoints

Each year, Semiconductor Digest turns to industry leaders and analysts to get their viewpoints on what they expect to see in the coming year in terms of critical tech and business trends. Hot topics continue to be artificial intelligence, cloud computing, energy efficiency, the supply chain, increased use of compound semiconductors, advanced packaging, 3D integration, chiplets and sustainability.

A Stronger, More Connected Semiconductor Industry in 2026

JOE STOCKUNAS, President, SEMI Americas

The semiconductor industry heads into 2026 with real momentum. Through the first three quarters of 2025, equipment billings came in just under 100 billion dollars. That is a record for this point in the year and a clear sign of the strength of demand. Companies continue to invest in leading-edge logic, DRAM, and advanced packaging to support the rapid growth of AI workloads, and that investment is carrying straight into 2026.

JOE STOCKUNAS

AI is changing the industry faster than anything we have seen in a long time. It is not only driving demand for compute and memory, it is changing what systems need to look like. Power efficiency, heat management, and interconnect density are now front-end considerations, not afterthoughts. These requirements will influence where companies choose to add capacity and how they prioritize capital spending in the year ahead.

Packaging will be one of the most important areas to watch. Chiplet and 3D integration are now moving into higher-volume production, and packaging has become a strategic part of system performance. We are seeing more investment in this area than ever before, but demand is rising just as quickly. The companies expanding their advanced packaging capabilities are putting themselves in a strong position for the next wave of AI and high-performance computing growth.

Global investment patterns also continue to shift. The United States, Europe, China, Taiwan, Korea, Japan and other regional hubs are all making moves to strengthen manufacturing and reduce risk in the supply chain. Even in a growth cycle, companies are managing a more complicated landscape and planning further ahead to keep operations resilient.

Workforce remains one of the biggest challenges. New fabs are ramping across several regions, and the talent pipeline is simply not growing at the same pace. Training, apprenticeships, and deeper partnerships with academia are essential. This is not a single-company issue. It is an ecosystem issue, and it needs to be addressed that way.

Looking ahead, 2026 will be another strong year for the industry. AI, datacenters, and high-performance computing will continue to lead demand. The opportunity is there, but meeting it will require preparation, collaboration, and steady investment. SEMI will continue to support the industry with the data, standards, and connections needed to keep this momentum going.

AI is in the Driver's Seat for 2026

DEAN FREEMAN, Technology Advisor, Kiterocket, a Southwest Strategies Company

In 2025, AI demand accelerated chip revenue beyond expectations. Advanced logic and DRAM both saw strong growth as AI adoption expanded across hyperscale and enterprise computing. Automotive, industrial, and consumer markets experienced mixed results in 2025 but will end the year slightly positive.

In 2026, according to the World Semiconductor Trade Statistics (WSTS), AI demand will drive semiconductor revenues to $975 billion. Logic tied to AI is expected to continue seeing strong growth. At the same time, the memory markets are tightening. Hynix and Micron have sold out HBM memory for 2026, while DRAM for compute and mobile phones is also in short supply. Due to the strong demand, the DRAM supply has been constrained, increasing memory pricing and pushing revenues to record levels.

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While all 3 major DRAM suppliers have new fabs coming online, it appears they will be managing how fast they ramp these fabs in order to maintain a longer period of profitability. Micron has even announced that it will be discontinuing a consumer line of DRAM in order to support the more profitable sectors. The higher pricing will help drive the semiconductor revenues to new heights, possibly exceeding the $975 billion forecast.

Additional revenue drivers are coming from the advanced packaging sector, where TSMC is expanding its CoWoS capacity from 61,000 wafers per month to more than 100,000. This added capacity will support AI accelerators and other advanced compute chip sales in 2026.

DEAN FREEMAN

Beyond AI, the industrial, consumer, and automotive sectors should see a recovery in 2026. Power management chips supporting both compute systems, as well as the grid infrastructure for hyperscale datacenters, should see a moderate increase in 2026. WSTS forecasts the automotive segment to recover and grow near seven percent in 2026. Although both automotive and consumer segments will depend on whether the consumer can stomach the increase in pricing of mobile phones, PC's, and other electronic devices due to the increase in memory costs.

Semiconductor equipment spending in 2026 will be led by AI logic and memory. The hope is that these sectors will offset the decline in revenues from China. Wafer fabrication equipment revenue is projected near $130 billion, depending largely on the pace of DRAM capacity expansion.

Ultimately, success in 2026 hinges on continued AI growth and hyperscale datacenters, which remain constrained by available energy supply and the workforce needed to build and operate new facilities.

Navigating the AI Boom in 2026

ANAND JOSHI, Technical Fellow, TechInsights

Artificial intelligence (AI) is everywhere, and it will remain the dominant theme in semiconductor manufacturing well into 2026. Currently, data centers and cloud computing are where the majority of AI models are being run, and the race is on to build the largest and smartest AI model. We expect this trend to start diverging in 2026 and the AI models to start shrinking in size, making them amenable to a range of devices.

Nevertheless, edge AI chip market ramp up is expected only after the model size starts shrinking. Our market research shows the smart home and tablet edge market rely heavily on cloud processing today due to easier upgrade capability, faster feature addition and monetization. This reliance on the cloud has vastly benefited hyperscalers and has given rise to a range of small 'neo-cloud' companies that focus primarily on AI services.

Computing performance needs in AI datacenters are doubling every six months, thanks to exponential growth in AI workloads. High power consumption of GPUs is propelling the power semiconductor market, particularly the data center segment, which is estimated to reach $4 billion in 2026. As such, gallium nitride (GaN) is gaining interest for high-efficiency, lower-capex applications, and is expanding into data center power supplies. As the GaN industry adjusts to this shifting landscape, the redistribution of manufacturing capacity and IP control will be a critical dynamic. 2026 is shaping up as a pivotal year for how value flows across the fabless, IDM, and foundry ecosystems. TechInsights expects the overall GaN market to be north of $900 million by 2026.

New approaches in manufacturing

To support growing demand for high-performance AI processors, companies are investing in advanced semiconductor manufacturing and packaging technologies. Majority of the AI accelerator chips today are in 4 and 3nm node, and we expect the first 2nm-generation design to hit the market in 2026, with anticipated production of over 500,000 wafers.

High-bandwidth memory (HBM) has become essential for high-performance AI in 2025. Despite high costs and yield challenges, we expect more HBM packaged into each AI chip in 2026.

While semiconductor packaging remains a hot area of investment driven by AI chips, the limitations of traditional organic substrates will become more pronounced in 2026, leaving glass as the preferred alternative material to combat warpage under high temperatures, coefficient of thermal expansion (CTE) mismatch, and scaling challenges. Similarly, we expect adoption of rectangular panel-level packaging to optimize efficiency and throughput of advanced processes across market segments, including AI. To reduce the power consumption in data centers, we expect co-packaged optics (CPOs) to become commonplace starting 2026. CPOs have shown that they can reduce power consumption in data center-scale AI systems by up to 3.5X.

ANAND JOSHI

China is catching up

In efforts to establish dominance in the global semiconductor technology industry, the US has introduced a series of sanctions in recent years to restrict China's access to advanced semiconductor design and manufacturing technologies. Nonetheless, Chinese firms continue to demonstrate notable technological progress, both

by expanding production capacity and by strengthening domestic supply chains. TechInsight's research suggests that China is already able to produce technology beyond 7nm. China is also closing the gap in terms of the number of AI models with US, having released around 40% of all models launched worldwide so far.

US companies, nevertheless, are likely to continue selling custom-created chips to China in 2026 that overcome performance and feature restrictions imposed by the American government. China market sales for AI chips are projected to increase in 2026, following a decline in 2025.

Summary

In 2026, we'll continue to see AI accelerate innovation, while the rest of the market remains flat by comparison. Traditional technologies are increasingly unable to meet the power, performance and scaling demands of AI semiconductors. Expect the biggest tech stories of the new year to solve these packaging, power and memory bottlenecks.

2026 Forecast: Cautiously Optimistic, but Highly Uncertain

MALCOLM PENN, Founder & CEO, Future Horizons

Q3 2025 delivered one of the strongest growth quarters on record, surpassed only by Q3 2009, lifting full-year 2025 growth to 22 percent. However, this performance reflects a tale of two markets. Growth was heavily concentrated in AI infrastructure and HBM memory, not traditional end markets such as smartphones, notebooks, wearables, TVs, and automotive.

Critically, growth was ASP not unit driven. IC unit volumes have yet to recover. While 2025 may appear to resemble a supercycle, it does not represent a broad-based industry recovery.

Looking ahead to 2026, the outlook is cautiously positive—but highly uncertain.

The primary risk is a slowdown, or even a pullback, in hyperscale data center investment. Investors are already voicing concerns about unclear revenue visibility, cash-flow, and the potential for overinvestment. At the same time, the long-anticipated recovery in non-AI markets remains elusive. Global economic headwinds, geopolitical uncertainty, and a lack of compelling new features continue to suppress demand, with no clear inflection yet in sight.

Key questions remain unresolved: when unit growth will resume, whether ASPs can continue to rise, and how non–bleeding-edge CapEx—particularly in China—will impact supply-demand dynamics. These factors

collectively drive an unusually high level of uncertainty for 2026.

Just as the COVID-19 pandemic fueled the 2020 boom and the subsequent 2022 collapse, AI enthusiasm has powered the 2025 surge. Entering 2026, the risk of a similar correction cannot be ignored. If AI demand moderates and other markets fail to rebound, today's primary growth engine could quickly become tomorrow's biggest vulnerability.

AI-driven optimism has pulled forward forecasts for a US$1 trillion semiconductor market by three years, to 2027. We are skeptical of these projections. Given the industry's well-established cyclicality, a downward correction appears inevitable. The current growth profile is narrow and fragile.

On balance, assuming no major shocks, we expect the chip market to grow approximately 12 percent in 2026. What we are far less confident about is the sign. If AI infrastructure growth collapses and the global economy slows, 2026 growth would be negative 12 percent.

Our overall message is clear: do not be distracted by headline dollar growth. Much of today's strength reflects ASP expansion rather than fundamental demand. Cracks are already emerging in the seemingly insatiable AI LLM ecosystem and the economic outlook uncertain. A true, sustainable semiconductor supercycle is unlikely before 2029, and strategic planning should proceed with extreme caution.

Sunny with a Chance of Occasional Showers

TIM HEGER, President, Chamber Solutions Division, Edwards Vacuum

The current outlook for semiconductor manufacturing remains positive. We anticipate steady progress in high-performance sectors – AI, cloud computing, and advanced logic nodes – even as some temporary softening continues in consumer electronics and EV sectors. The surge in AI investment is supporting demand for leading-edge technologies and contributing to gradual increases in wafer prices. Data center expansion to accommodate AI and cloud computing is expected to continue over time. Sustainability and energy efficiency are becoming increasingly important as semiconductor manufacturers work to manage operational costs and environmental impact. At the same time, sustainability concerns are emerging around the power consumed by semiconductors in use.

TIM HEGER

As semiconductor manufacturing processes become more complex, vacuum and abatement systems are increasing important for maintaining process stability, yield, and sustainability. The industry's focus on energy efficiency and environmental responsibility aligns with the capabilities of modern vacuum solutions, making them critical enablers of future growth. We also see a growing opportunity in advanced packaging applications where the increased complexity of chiplet architectures and 3D integration are driving the need for fab-like vacuum solutions in bonding, stacking, and encapsulation.

Within Edwards we are focused on:

- **Next-Generation Pump & Abatement Innovations** – including new dry pump platforms that offer significant improvements in footprint, energy efficiency, water consumption, and nitrogen usage; new turbomolecular pumps that deliver higher pumping speeds from smaller footprints with better energy efficiency; and next generation compressors that optimize energy efficiency in the subfab. Upgrading abatement systems in our customers' existing install base delivers greater total energy savings than focusing only on new equipment. Retrofits in legacy fabs drive significant efficiency and sustainability improvements at scale. This approach maximizes impact across both new and established facilities.
- **Predictive Maintenance** – using AI driven models and enhanced sensor data to anticipate maintenance requirements, synchronize service procedures with other required tool maintenance, avoid unplanned downtime, reduce scrap costs, and minimize risk of process tool damage.
- **Localized Service Support** – expanding our global network of service and technology centers for faster response and lower travel-related carbon footprint; leveraging local knowledge and established relationships to promote equipment upgrades that reduce carbon footprint, especially in legacy fabs, the largest portion of our installed base.
- **OEM Partnerships** – collaborating closely with leading equipment makers and emerging players where co-development ensures optimized performance, energy efficiency, and environmental compliance.
- **Sustainability** – A significant share of the total energy usage in a fab is consumed by our products in the subfab. Clearly, improvements in energy efficiency there can have a significant impact on the total. Moreover, this is one of those happy circumstances where environmental and economic drivers align. Improvements in energy efficiency reduce both emissions from purchased power and the operating cost of those purchases.

Less direct but potentially far more significant are reductions in Scope 3 emissions from power consumed by vacuum and abatement systems in use.

Only 4 years ago, in our contribution to the Semiconductor Digest 2022 forecast, we cited an observation from the Decadal Plan for Semiconductors by the Semiconductor Research Corporation that at current growth rates power consumed by computing was on track to exceed global energy production sometime between 2040 and 2050. And that was before the current boom in AI. We are already seeing this issue enter the public consciousness as communities struggle to share power resources equitably between computing centers and other individual, corporate, and institutional consumers. Even in this arena sophisticated technologies in the sub fab will play a critical role in supporting advanced processes and architectures that improve the energy efficiency of computing, such as our current support for the advanced lithographic technologies used to create nanoscale devices.

Industry Transformation and Innovation in 2026

JOHN MACULLEY, Global High Tech Industry Strategist, Dassault Systèmes

JOHN MACULLEY

The semiconductor industry is undergoing an exponential transformation, driven by rising complexity, emerging technologies, and shifting global demand. Advanced process nodes are projected to achieve 2 nm by 2025, with research targeting angstrom-level precision. Looking ahead to 2026, innovations like 3D packaging, quantum computing, and AI accelerators are shaping the next generation of chips, while executives focus on reducing costs and accelerating time-to-market.

- **Increased AI-driven design & manufacturability:** Coordinating equipment development with chip designs, process technologies, and materials is increasingly critical for faster time-to-yield and improved system-level reliability. In 2026, we expect that AI-driven virtual twin simulations and Model-Based Systems Engineering (MBSE) approaches will enable companies to optimize designs digitally, design for manufacturability, reduce reliance on physical prototypes, and improve systems performance.
- **Geopolitics, supply chain & ecosystem collaboration:** Restricted access to advanced chip-making technologies and global supply chain pressures are creating four distinct and sovereign semiconductor ecosystems in the U.S., Europe, Asia, and China. In 2026, collaboration, technology co-optimization, and integrated platforms across these ecosystems will be essential to ensure resilience, security, and competitive advantage.
- **Surging demand for AI and High-[Performance Computing, IP management:** Rising demand for AI accelerators, such as GPUs, and high-performance computing is driving a focus on energy efficiency, thermal management, and system-level performance. Looking forward, fully integrated, cloud-based engineering platforms will help manage data, protect intellectual property, maintain traceability, and reduce costly misalignment or late-stage revisions across organizations and value chains.

Edge AI Reaches Its Scalable Future

MARK REITEN, Corporate Vice President, Licensing, MPD and EAI Business Units, Microchip Technology

The edge AI landscape is evolving faster than ever, and 2026 will be the year organizations shift from proof-of-concept thinking to full production deployment. Across every major market segment, engineering teams are moving beyond experiments and adopting edge intelligence as a foundational part of their system architecture. This shift is driven by clear improvements in performance, power efficiency, security and the availability of tools that simplify development on resource constrained devices.

MARK REITEN

Companies have spent the past several years evaluating how AI can improve reliability, reduce operating costs and strengthen user experiences. In 2026, the focus will swing toward operationalizing these ideas. Designers are selecting embedded processors, MCUs, FPGAs and MPUs capable of running inference close to the sensor with consistent performance and predictable power draw. Success at the edge will come from solutions that pair the right compute with streamlined developer tools and the long product life cycles needed to support multi-year platforms. Strong technical and FAE support will also play a critical role as teams look for suppliers who can guide them through both AI concepts and practical system constraints.

The industry is moving away from large, generic models and toward tightly optimized networks tailored for low-power devices. Quantization, pruning and architecture search are becoming standard practice as engineers seek models that fit within kilobytes or a few megabytes while still delivering the accuracy their applications demand. Toolchains that simplify optimization, compression, evaluation and deployment will accelerate this trend throughout 2026, especially when paired with compute platforms that are easy to use and supported by reliable, long-term software ecosystems.

Keeping data local provides inherent

privacy advantages, and 2026 will bring even stronger requirements for hardware-based security. Root-of-trust, secure boot, encrypted storage, and protected execution will become baseline expectations as customers demand trustworthy inference and reliable model integrity. With many edge devices expected to remain in the field for a decade or more, long-term support and secure firmware update paths will be essential.

Power efficiency will continue to be one of the strongest decision drivers. Metrics like inference-per-second-per-watt will guide device selection as companies work to reduce cloud traffic, manage operational costs and lower their carbon footprint. Edge AI's ability to process data locally provides a measurable sustainability advantage by minimizing data transmission and extending battery life in mobile and remote systems.

In 2026, edge AI will mature into a dependable, scalable part of modern system design. With optimized models, secure hardware, low-power performance and strong long-term support, the industry is ready to move from exploration to real production at the edge.

Power Efficiency and Reliability Redefine Memory Requirements in 2026

SANJEEV AGGARWAL, CEO, Everspin Technologies

2026 is the year of memory. It will move from its traditional supporting role to being acknowledged as a determining factor in system design. As workloads grow across edge inferencing, industrial automation and satellite communications, the limitations of traditional memory are harder to ignore. Power, performance and reliability are now as critical as capacity, and that shift is bringing persistent memory technologies to the forefront.

SANJEEV AGGARWAL

Across every market we track, power has become the dominant requirement. AI systems that once relied almost entirely on processor performance are now constrained by the energy demands of the memory subsystem. This is where MRAM's value stands out. Its ability to retain data with virtually no standby power and wake in less than a second is meaningful for devices operating at the edge. A sensor or camera no longer needs to stay active waiting for an event. It can remain off, wake instantly, process locally and avoid the cost and delay of returning to the cloud. When customers evaluate the entire solution, including the power envelope, MRAM is one of the economical choices.

Industrial automation remains one of the strongest growth areas. Modern production lines need deterministic, instant-on behavior when power is interrupted. With higher-density MRAM, programmable logic controllers and robotics platforms can store more state data at higher bandwidth. As factories automate more functions, this requirement only becomes more important.

Aerospace and defense programs are seeing similar dynamics. Low Earth orbit satellites have limited time to exchange data with ground stations. They cannot wait for long write times or risk corrupted updates. That is exactly where MRAM fits. It gives them a reliable configuration memory that does not degrade unlike other non-volatile memories do under repeated writes or radiation exposure.

We're also seeing changes in how people think about interfaces. They are moving away from traditional parallel interfaces because of the area penalty, and most new designs need more bandwidth. Octal SPI offers 400 MB per second, and we are seeing early work around low-power DDR interfaces as teams look for more speed while keeping power in check.

Going into 2026, the biggest shift we expect is that memory is stepping into a more central role in system planning. Designers are no longer asking only about cost and density. They are asking how quickly they can update a device, how long it will hold data without power, and how it behaves after millions or billions of cycles. Those questions point directly to persistent, high-endurance solutions. As power and reliability continue to define the boundaries of system performance, we expect MRAM to be part of more platforms that were never considered candidates a few years ago.

2026: Power Delivery Defines Both Limits and Opportunities

EELCO BERGMAN, Chief Business Officer, Saras Micro Devices

It's hard to argue that, as we head into 2026, there is strong momentum in advanced compute, particularly for the AI data-center market. But we are also facing an increasingly unavoidable reality: System performance is no longer limited by transistor capability alone. The combination of increasingly powerful processors and accelerators fabricated on next-generation process nodes, higher levels of silicon integration, and rapid adoption of heterogeneous packaging is pushing power-delivery requirements to the edge of what current architectures can support.

EELCO BERGMAN

As devices move into newer process nodes and into 2.5D and 3D configurations, we see a sharp rise in localized power density inside the device and package. More silicon

activity is being concentrated in smaller areas, while the high current distribution paths are becoming longer and more intense. That combination puts additional load on the power-delivery network. Loss mechanisms that were previously absorbed in the margin begin to show up in ways that affect temperature, transient behavior, and long-term stability.

These technical pressures do not exist in isolation. The timing mismatch between compute demand and electrical infrastructure expansion is the root of the industry's need for higher efficiency. AI processors are approaching multi-kilowatt power levels, AI compute system racks are on a path to megawatt power levels, and at the same time, data-center operators face limits on how much new capacity they can bring online. In practice, this means the power budget becomes a real boundary condition for large-scale deployment.

It is these constraints that force the industry to focus on shifting toward architectural adjustments rather than incremental tuning. More design work is moving into device-package co-optimization, supported by electrical-thermal-mechanical co-simulation. Vertical delivery paths, performance embedded passives with higher density, and improved power-ground structures give designers more control over current distribution and fast-load events. These changes reflect a broader need to rethink how power is moved and stabilized within advanced packages.

The common theme is that power delivery is now a central design element, not a secondary one. Teams that recognize this and approach compute performance, thermal behavior, and PDN design as an integrated problem will be in a stronger position. This will be the trend for 2026, but the pace of that progress will track directly with how effectively these power-delivery constraints are addressed.

Regionalization: The End of Global Semiconductor Supply Chains?

BARRY O'DOWD, Barry O'Dowd, Global Head of Semiconductor Development, Kuehne+Nagel

BARRY O'DOWD

The past few years have been marked by constant disruptions, making unprecedented conditions and shifts in the semiconductor industry the norm. While predicting what comes next is impossible, one trend remains clear: Regionalization is gaining even greater momentum in 2026. This shift, although not new, will accelerate as more fabs are deployed and built, reshaping global supply chains.

As regionalization continues, semiconductor businesses are increasingly focused on ensuring smooth and efficient regional logistics operations. Yet international trade lanes remain vital. While activity undertaken within the region is expected to increase, the journey to a completely self-sustained regional supply chain will remain a long one. Asia, in particular, will continue to play a significant role in supply chains worldwide. For example, it continues to dominate back-end packaging activities in origins such as Taiwan and Malaysia, ensuring that global interdependence in the semiconductor supply chain will persist for some time.

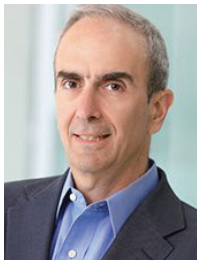
Within this environment, not only is access to a regional and global shipping network vital, but also the ability to adapt focus and adjust routing quickly. Recent times have proven that agility and resilience are more crucial than ever. Semiconductor companies need a logistics partner with a robust global reach to manage both local and international flows. This requires a supply chain built on smart planning, priority handling at hubs to minimize delays, real-time visibility, proactive monitoring, continuous stakeholder communication, and rapid response to disruptions.

With digital solutions delivering actionable insights and experts guiding you every step of the way, you can stay ahead of expected and ready for the unexpected. The market may be constantly changing, but with the right partner, your semiconductor supply chain can stay strong, agile and future-ready.

Resilience in 2026 isn't about choosing regional or global, it's about mastering both. The winners will be those who can localize execution while staying globally connected.

AI-Driven Collaboration and Smarter Decision Making throughout the Supply Chain in 2026

JOHN KIBARIAN, CEO, PDF Solutions



JOHN KIBARIAN

The burst of semiconductor manufacturing capacity is welcome news for 2026 now that 18 new fabs construction projects got started in 2025. Meanwhile, AI pushes demand in cloud, data centers and at the edge as the industry evolves into the era of 3D. This is driving the path to $1T revenue before 2030. AI cloud and edge applications alone could represent 67% of the market.

Optimism for this growth should be couched with caution. The viral effect of added capacity, AI and 3D has created manufacturing and R&D challenges that must be addressed. An AI-based unified data and collaboration infrastructure across the entire supply chain could do just that.

Advances in AI-based 3D chiplet and system design and manufacturing innovation are critical as the industry moves toward complex hybrid packages.

In 2026, managing an expanded and complex global supply chain will be accomplished with AI-driven collaboration.

It's important to note that the semiconductor industry has always thrived on collaboration and innovation. That has not changed, though the definition of collaboration has expanded from just referring to partnerships. It now reflects the ability to leverage AI at all levels of the ecosystem for real-time data sharing and multi-party cooperation, securing data networks, improving operational efficiency and cost and increasing supply chain resiliency.

Challenges noted above will continue to be resolved in 2026 by fundamentally reimagining the current reactionary model into streamlined AI-based, mission-critical platforms sharing data, orchestrating operations and deploying intelligence across increasingly complex global supply chains.

Growing design and manufacturing costs throughout the semiconductor supply chain necessitate the transition to the infrastructure of the future and the need for analytics to drive efficiency. Starting in 2026, the industry will begin to see the results of AI-driven collaboration to enable smart decision making, bridging hundreds of sites and organizational systems across the globe, enabling seamless and protected information sharing.

Packaging and Interconnects in the Spotlight

STEVE WOO, distinguished inventor and fellow at Rambus

As compute gets faster each generation, the industry is fighting an uphill battle as package sizes grow and greater numbers of chiplets and HBM stacks and other memories are integrated into larger super chips. Packaging and IOs will further entrench themselves as important enabling

STEVE WOO

technologies and key citizens in chip and system architecture designs. Performance, power-efficiency and reliability for I/O designs and pin-field engineering will grow in importance as data movement requirements dictate bandwidth needs, which in turn impact physical design constraints, power delivery, and thermal management.

Memory supply bottlenecks inside and outside the data center

Data center investments continue to rise with AI, and in particular agentic AI. Greater demand will put pressure on supply chains as data centers consume more memory. Non-data center markets will face headwinds in memory supply as a result.

Memory will be in focus as applications consume higher capacities and bandwidths, driving demand for newer DRAM technologies like HBM4 and GDDR7 as they ramp. Higher capacity and bandwidth memory technologies like stacking, multi-PAM signaling, and CXL-attached pools will see growing interest and adoption to keep accelerators and other computing infrastructure fully fed with data.

Inference to get dramatically cheaper

Inference gets dramatically cheaper and more capable, enabling agentic AI to move into edge systems where designers must balance performance with robust security.

- **Advances in Specialized Silicon —** Purpose-built accelerators and optimized architectures for AI inference are reducing cost per operation, making high-performance inference increasingly viable outside of hyperscale data centers.
- **Energy Efficiency Gains —** Improvements in power consumption per inference task means edge devices can run more sophisticated models without prohibitive thermal or battery constraints.
- **Economies of Scale and Process Shrinks —** Mature 3nm and emerging 2nm nodes, combined with chiplet-based designs, will drive down costs while maintaining application performance targets.

On-device AI becomes a default design choice ("mixed compute" is the new cloud)

By 2026, most premium PCs and phones will ship with NPUs at approx. 40–45 TOPS and OS features that include **local inference** for speed, privacy, and cost control—while bursting to the cloud for heavier jobs. Microsoft's Copilot+ PC program (Windows 11, NPUfirst features) and Qualcomm's Snapdragon X platforms demonstrate the hardware baseline; Apple's **Apple Intelligence** roadmap expands **ondevice LLMs**, Live Translation, visual intelligence and developer access to the local foundation model.

Expect **privacycentric**, **batteryefficient** experiences (search, transcription, image editing, offline copilots) to become table stakes, with enterprise policy deciding what runs on device vs. in cloud.

Preparing for the Next Wave of Compound Semiconductor Scale-Up

ANIL VIJAYENDRAN, VP, Product Line Management, Veeco

As we look toward 2026 and beyond, several technology inflections are reshaping the trajectory of compound semiconductors—and positioning Veeco for an important new phase of growth. The most significant momentum is building around gallium nitride (GaN), driven by demand for

more efficient power conversion in data centers and electrified systems. GaN adoption is accelerating, with production beginning to shift to 300mm wafers, which will ultimately deliver the lowest-cost manufacturing option. We are thus entering 2026 with a strong position in 300mm for our Propel 300 GaN MOCVD product.

Photonics is another area where we anticipate substantial progress. Indium phosphide (InP) lasers remain increasingly important for hyperscale data center infrastructure, and Veeco has already secured key wins in this space while actively competing for additional customers. As AI continues to reshape cloud architectures, both GaN and InP will play critical roles in enabling higher-performance, lower-power optical and electrical interconnects.

ANIL VIJAYENDRAN

MicroLEDs also continue to advance, particularly for augmented reality (AR) glasses, high-end TVs, and smartwatches, further broadening opportunities for our Lumina MOCVD platform. While manufacturing has not yet reached volume, pilot lines are expanding to address resolution and power-efficiency requirements. The industry is watching leading AR platforms closely and preparing for broader adoption as costs come down. We see 2026-27 as seeding years for microLED, laying the foundation for broader commercialization in 2028-29.

Across these markets, forecasting demand remains one of the biggest challenges in the compound semiconductor ecosystem. Unlike silicon nodes—where roadmaps are well defined—compound semiconductor devices evolve based on performance and cost, and transitions such as the move to 200mm and 300mm wafers require adapting front-end methodologies to III-Vs. Regardless of the end market, lowering cost across the value chain is critical.

Success in 2026 will depend on strong customer partnerships, deep alignment with roadmaps, and the ability to scale with the right technologies at the right time. Veeco is laying this groundwork today—strengthening its MOCVD portfolio, advancing next-generation epitaxy platforms, and positioning with customers as they prepare for future high-volume ramps.

The Entirely Curvilinear Photomask Era Has Arrived

AKI FUJIMURA, CEO, D2S

Moving into 2026, semiconductor manufacturing has reached a curve in the road – one driven by the convergence of GPU acceleration, pixel-based computing, eBeam multi-beam mask writers, and entirely curvilinear inverse lithography technology (ILT). Exploratory work at organizations like imec and Micron has evolved into an industry-wide movement. The consensus is growing: *entirely curvilinear photomasks are not only possible, they're inevitable.*

In the mask shop, from ILT to mask process correction (MPC), every stage of the manufacturing chain is being reshaped by the ability to process and optimize true curves. Entirely curvilinear masks use *only shapes that can be manufactured*. When you use mask shapes that can actually be manufactured, the mask you design is the mask that prints. This transition from rectilinear Manhattan geometries (which do not print as true rectangles) to entirely curvilinear features embraces the inherent smoothness of the natural world – where 90° angles don't exist – to unlock the potential of curves for improved performance and efficiency in silicon.

D2S has invested in the shared vision for an entirely curvilinear mask ecosystem for over 16 years. GPU acceleration has broken the computational barriers that once made entirely curvilinear masks impractical. D2S is a key player in the revolution enabling the industry's transition to entirely curvilinear manufacturing by offering GPU-accelerated, pixel-based solutions for computing entirely curvilinear masks (TrueMask® ILT), and for computing MPC for entirely curvilinear masks (pixel-level dose correction, or PLDC). D2S TrueMask ILT enables you to ask for manufacturable curves and with D2S PLDC you get the mask you ask for. These solutions demonstrate how GPU-acceleration and pixel-based computing can turn complex mask shapes into manufacturable realities, written by shape-agnostic multi-beam mask writers. The results are not just better masks, but wafers with enhanced yield and reduced variability.

Micron's leadership in applying both ILT and PLDC technologies, most recently recognized for a best paper award at the 2025 Photomask Japan conference, has helped legitimize curvilinear ILT as a cornerstone of next-generation lithography. Their work shows that the advantages of an entirely curvilinear mask ecosystem extend far beyond theory. Meanwhile, Tekscend Photomask was awarded best poster at Photomask Japan for demonstrating PLDC benefits in mask manufacturing for their customers.

2026 will be remembered as the year when "curvy masks" moved from conference slides to production lines. GPU acceleration, multi-beam mask writers, and an entirely curvilinear mask ecosystem have made the aspirational achievable.

The next generation of semiconductors will be shaped by the elegance of curves.

More Layers, More Power, New Problems: The Metrology Revolution Behind 3D Chips

JOSÉ MANUEL RAMOS, CEO, Wooptix

JOSÉ MANUEL RAMOS

We've seen important developments over the past year in new architectures for chip design that improve performance by taking advantage of 3D techniques to pack more layers into each wafer. One of the trends that could change the way chips are manufactured is the rapid evolution of backside power delivery networks (BSPDN) for logic and 3D DRAM.

Optimizing the space within the wafer to implement better distribution of its components is a key approach to increasing chip performance. While 3D DRAM memories provide faster access to data, BSPDN enhances efficiency by placing the power delivery network on the backside of the wafer, achieving lower power consumption and boosting chip performance.

In 2026, we'll likely see major advancements in increasing the number of layers that can be placed on the wafer. However, this comes with a very important concern: Adding more layers places greater pressure on the wafer, which can lead to distortions in the dies, making them unusable. In addition, the new processes required to deposit so much inside such a small space are very costly—each chip lost due to warpage comes with a steep price.

For semiconductor metrology, this presents both a challenge and an opportunity. Demand is rising for new metrology systems capable of measuring complex advanced packaging architectures, especially when it comes to warpage, which greatly affects the device properties and downstream processes. 2026 will be a year of innovation in metrology, with a focus on developing new approaches that can deliver highly detailed insights into the new generation of chip architectures.

In particular, we expect to see developments coming from Europe. The European Union has put significant effort into developing policies and investing in creating a strong semiconductor ecosystem within its member states, promoting cooperation between public institutions and private companies.

Precision Motion Plus Light: MEMS Photonics and Optoelectronics in 2026

ALISSA M. FITZGERALD, Ph.D., CEO of A.M. Fitzgerald & Associates

ALISSA M. FITZGERALD

Reducing the massive amounts of electrical power consumed by AI data centers and improving data bandwidth has motivated a sea change in data networking: Fiber optic bundles are replacing copper wiring, and optical circuit switches (OCS) are replacing electronic network switches. In 2026, we'll see increasing focus on photonics as the fundamental infrastructure technology for modern data centers.

Photonics makes sense for efficient networking on so many levels. By flowing data between computer racks as photons instead of as electrons, the power loss in electrical current flow (Joule heating) is eliminated. This reduces data center power needs by a remarkable 30-40%. And optical wavelength division multiplexing (WDM) superposes multiple data streams to allow the massive data throughput needed by AI applications.

Photonics needs nanometer- or micron-scale motion to modulate light, and MEMS offers precision motion in the form of electrostatic or piezoelectric actuators. While hybridized MEMS and photonics technologies have been developed in academic groups around the world for years, the massive market pull of AI data centers is now motivating their commercialization. Other complex systems needing high data bandwidth, such as autonomous vehicles or medical image analysis at enterprise scale, will soon enjoy collateral benefits from the data center-driven confluence of photonics and MEMS.

Two emerging applications are:

- **To Couple, Switch or Tune Photonic Integrated Circuits** — As optical systems in telecommunications and data networking continue to scale in complexity, the ability to efficiently and rapidly couple, switch, and tune with precision in a photonic integrated circuit (PIC) becomes critical. Expect to see thin-film piezoelectric materials, including PZT and emerging lead-free films such as KNN, pack high actuation force into a small volume and perform acousto-optic modulation at gigahertz frequencies.
- **Optical Beam-Steering and Multiplexing** — Free-space optical systems need components capable of fast and power-efficient surface redirection to steer laser beams. These types of systems are in highest demand for data center optical switching and automotive LiDAR. Expect to see more MEMS beam-steering mirrors, which have been developed and commercialized over the past two decades — primarily for visual display applications — offer microsecond response times, large optical apertures and scalable high-volume manufacturing.

Years of academic research, mature MEMS technologies available and compatible for integration, scalable

photonic-MEMS manufacturing ready-to-go, and strong market demand from data centers are in alignment to produce an exciting new wave of products: integrated MEMS-photonic devices.

Precision motion plus light equals new solutions for data center networking, LiDAR systems, photonic computing and many other advanced applications.

Optical MEMS Boosts the Microphone in 2026

KIERAN HARNEY, CEO, sensiBel

Across mobile devices, conferencing solutions, spatial recordings, and AI-driven interfaces, the demand for higher-performance audio capture is clear: Systems need microphones with dramatically lower noise, higher overload capability, and tighter part-to-part matching to support multi-microphone beamforming and advanced signal processing. Yet the traditional capacitive and piezoelectric MEMS microphones that have dominated the industry for the past twenty years have made incremental gains at best. Saddled by fundamental architectural constraints — micron-scale diaphragm gaps, squeeze-film damping, backplate noise, and mechanical clipping — these older microphones limit both signal-to-noise ratio (SNR) and dynamic range.

KIERAN HARNEY

In 2026, this will change as optical MEMS microphones deliver the first high-fidelity audio capture for consumer, prosumer, and studio applications.

Optical MEMS devices are free from the structural constraints of capacitive and piezo MEMS technology. Having replaced the capacitive readout with an interferometric optical detection system in its SBM100 series microphones, sensiBel will begin volume production of a new category of MEMS microphone that breaks through longstanding performance ceilings.

With 80 dB SNR, a 14 dB noise floor, and a 146 dB SPL acoustic overload point (AOP), sensiBel's optical MEMS mic achieves a 132 dB dynamic range — a 20+ dB leap past today's best capacitive solutions. The technology's mechanical architecture, with diaphragm separation in the tens of microns, eliminates squeeze-film noise and prevents stiction, enabling both exceptional low-noise sensitivity and virtually unlimited diaphragm movement.

These performance gains do more than improve audio quality; they simplify semiconductor system design. A highly linear 24-bit digital output (PDM, I²S or TDM) reduces signal-chain complexity and minimizes calibration overhead in multi-microphone arrays. Applications once hindered by microphone noise — such as 3D spatial audio, AR/VR capture, advanced ANC, AI voice interfaces, and edge-based sensing — now support redesigns with greater accuracy, robustness, and user immersion.

Looking to 2026, optical MEMS will expand beyond premium adoption. Ongoing development promises smaller packages and lower power and will support scalable high-volume manufacturing for consumer markets. As audio and acoustic sensing become increasingly critical to next-generation devices, optical MEMS is poised to become a foundational semiconductor technology — akin to the transition from electret condenser mics (ECMs) to capacitive MEMS more than two decades ago.

In an industry defined by breakthroughs, optical MEMS represents not just an incremental improvement, but the opening of an entirely new performance package.

Why RF's Future in 2026 Lies in the Third Dimension

PAOLO FIORAVANTI, CEO, Circuits Integrated Hellas

PAOLO FIORAVANTI

As we head into 2026, the radio-frequency (RF) segment of the semiconductor industry is poised for robust growth. Demand is being driven by advanced 5G deployments, expanding non-terrestrial networks (NTNs), satellite communications, and defense modernization programs. According to Fortune Business Insights, the global RF semiconductor market is expected to nearly double from about $25.6 billion in 2025 to $50.3 billion by 2032, underscoring sustained demand for RF solutions across applications.

Yet beneath these promising numbers lies a persistent technical challenge. Much of the RF industry today still relies on planar, 2D integration of discrete components — each optimized through incremental material and process improvements. While these efforts, such as scaling gallium nitride (GaN) and refining gallium arsenide (GaAs) performance, have extended capabilities, they are bumping up against the physical limitations of 2D architectures.

In typical RF systems, separate dies — for power amplification, signal processing, and control — sit side-by-side on a PCB and connect via wire bonds or long traces. At high frequencies, these planar interconnects introduce parasitic effects that degrade signal integrity and increase power loss. As RF designs push into the Ka-band, and millimeter-wave beyond, these inefficiencies become more pronounced. Simply put, we are building more capable transistors but connecting them with longer, lossy "wires."

The next leap in RF performance — especially for systems where size, weight, and power (SWaP) matter

— will come from heterogeneous 3D integration. GaAs optimizes linearity for front-end amplification; GaN delivers high power density; silicon excels at complex control and digital logic. Instead of placing these dies next to one another on a board, 3D integration stacks and vertically interconnects them using technologies such as system-in-package (SiP), through-silicon vias (TSVs), and advanced interposers.

The benefits are real and measurable:

- Greater interconnect efficiency: Microscale vertical vias replace millimeter-long traces, cutting interconnect power consumption by 30–50 %.
- Significant SWaP reduction: A stacked 3D RF module can shrink system footprint by 60% or more—a vital advantage for satellites and beamforming arrays.
- Improved signal quality: Shorter electrical paths reduce insertion loss and noise, boosting overall link performance.

This trend validates Circuits Integrated's focus on tightly integrated GaAs antenna-in-package (AiP) solutions. While GaAs remains the superior choice for high-efficiency, linear amplification in dense phased arrays, its full potential is only unlocked when it is tightly integrated—vertically—with silicon control layers. In the race toward 2026 and beyond, success won't come from the best standalone transistor: it will come from the best architected, vertically integrated RF system. The era of discretes is giving way to the era of 3D integrated RF.

Transitioning Advanced Packaging From "More Moore" to "More than Moore"

GUIDO UEBERREITER, VP Semiconductor Strategy, VON ARDENNE

For decades, the semiconductor industry has pursued a clear objective: to integrate as many functions as possible into a single system-on-chip (SoC). By scaling transistors from millions to trillions on a single die, the "More Moore" large-scale integration approach delivered remarkable technical and economic benefits, leading to technologies that enabled the PC, mobile phone, and the early stages of artificial intelligence (AI).

GUIDO UEBERREITER

Over time, it became obvious that not all functions on the SoC benefit from scaling in the same way. New megatrends require optimization on all fronts: the compute cores, memory subsystems, interfaces, as well as the power supply infrastructure.

Today this shift is most visible in high-performance compute, where we are witnessing a de-integration of monolithic SoCs and replacing them with heterogeneous, chiplet-based architectures. Functions that were once distributed across printed circuit boards and discrete packages are now brought into close proximity within a single advanced package to deliver higher bandwidth, lower latency, improved power efficiency and better cost control. "More than Moore"— value created by integrating diverse functions and technologies into a single package—has been critical to the performance and cost efficiencies that enable AI to scale today.

In 2026, we expect to see this architectural transition expand beyond compute. High-end radio frequency (RF) components will be co-packaged with data processing companion chips, similar to what we have been doing for decades with camera and image sensor solutions. Similarly, we will see power semiconductors being integrated with logic chips for better efficiency and system response. Photonic integrated circuits (PICs) will be packaged together with data processing chips to overcome electrical interconnect limits for better signal integrity.

Of course, economics need to benefit as well. The industry transitioned from wafer-level packaging to panel-level packaging to improve cost-efficiency. Similarly, heterogeneous integration offers an opportunity to combine chips from different wafer sizes and technology nodes and place them as close together as possible within a single package to maximize performance and yield.

VON ARDENNE's equipment portfolio is well positioned to support these advanced packaging roadmaps in 2026 and beyond. From cluster-based systems for wafer-level packaging, to panel-level equipment for larger package formats—VON ARDENNE enables high throughput, uniform, and scalable deposition and processing. These solutions support the ability to create and fill nanometer-level structures, regardless of substrate size or type, ensuring flexibility and quality as packaging architectures continue to evolve.

Advanced Packaging to Continue Making Major Strides in 2026

BYRON EXARCOS, CEO, ClassOne Technology

As the industry moves into 2026, advanced packaging remains one of the strongest engines of growth and innovation across the global semiconductor landscape. Demand continues to accelerate across AI, data center, photonics, and defense applications, creating persistent pressure for higher-performance interconnects, more precise metallization, and tighter process integration. These trends directly align with ClassOne Technology's core strengths in advanced plating, surface preparation, and wet

BYRON EXARCOS

etch processing, positioning us well to support the next wave of development activity around the world.

We are seeing particularly robust momentum in Europe, where investments in advanced packaging are turning on to support regional manufacturing production ramps as well as shorten technology-development cycles. Asia continues to be another key area of growth as customers scale both legacy and emerging packaging platforms. While the U.S. market remains steady, these expanding international investments are driving an increasingly global customer base for ClassOne.

At the same time, AI data-center buildouts continue to reshape the requirements for both photonics and advanced logic packaging. Our customers are actively ramping production of the next generation of transceivers, switches, and AI-centric devices—applications that depend on exceptionally uniform plating performance and seamless integration of downstream processes. Across these markets, we are seeing strong interest not only in our established Solstice platform but also in our new Solstice Max, which expands our reach into 300mm manufacturing. The system has been very well received, with multiple orders across regions, and we are focused on executing installations through the end of this year and into 2026.

We are also encouraged by customers who initially adopted our plating systems and are now expanding into surface-prep steps such as metal lift-off (MLO) and photoresist strip, as well as such additional wet-processing capabilities as under-bump metallization (UBM) etch and bevel etch. These engagements validate our strategy of delivering tightly integrated, single-wafer solutions that streamline process flow and support increasingly complex packaging architectures.

Looking ahead, we expect 2026 to be a year defined by continued investment, deeper collaboration with development partners, and strong execution on our growing pipeline. The long-term drivers for advanced packaging are firmly in place, and ClassOne is committed to supporting our customers as they scale for the next phase of semiconductor innovation.

Multi-Modal Workflows and AI Acceleration Are the Future of Failure Analysis

THOMAS RODGERS, Senior Director of Market Strategy, Head of Business Sector Electronics, ZEISS Microscopy

THOMAS RODGERS=

As semiconductor devices become more complex and densely integrated, the industry requires failure analysis (FA) approaches that involve orchestrated workflows. We are seeing more correlated, multi-modal approaches that combine non-destructive solutions for defect localization (high-resolution X-ray computed tomography, optical wavefront/phase imaging, thermal/infrared, and light and acoustic microscopy) with destructive solutions, such as focused ion beam (FIB) and transmission electron microscopy (TEM), being used for final analysis. In 2026, we expect to see enhanced use of artificial intelligence (AI) models that improve the speed and cost of these workflows. AI will increasingly get better at classifying failure types and their root causes to enable rapid triage and reduce the bottleneck of scarce, highly expensive analysis, such as TEM.

For example, hybrid bonding is promising because it enables chiplets and heterogeneous integration for advanced package systems. However, the range of Cu-to-Cu bond sizes is projected to push the boundaries to 400nm interconnection pitch. As a result, fault isolation and FA for IC packages involving hybrid bonds are expected to face more challenges.

3D X-ray microscopy (XRM) is an effective, high-resolution imaging and analysis tool used for non-destructive defect location, particularly in package-level failure analysis. Since XRM delivers submicron resolution, the emergence of novel high-density interconnect technologies challenges the resolution limit of traditional XRMs.

One approach is our 3D X-ray nanotomography technique that is capable of imaging with 50nm resolution. Using a multi-modal approach, the correlated FIB-SEM workflow follows to image interconnect structures or defects at precise fault regions with nanometer accuracy based on the 3D nanotomographic XRM data already acquired. Long scan times can be a limiting factor for XRM, so we utilized an AI-powered software, ZEISS DeepRecon, to speed up X-ray data acquisition by a factor of four. With appropriately prepared samples, the developed workflow enables successful and efficient FA from die metals, RDLs, and microbumps to hybrid bonds in complex IC packages. This approach successfully demonstrates the value of new multi-modal approaches.

Looking ahead, we foresee that these multi-modal datasets will fuel the development of AI-based predictive models capable not only of identifying defects and their root causes but also of forecasting their occurrence and underlying causes from the earliest symptoms.

Test as the Enabler of the AI Factory

SHANNON POULIN, President, Semiconductor Test Division, Teradyne

As we head into 2026, it's impossible to ignore that AI is shaping the future of our industry. The rapid build-out of

"AI factories" is changing how devices are designed, assembled and validated. These changes are elevating the role of semiconductor testing, in an ever-increasing quest to improve yield and reliability, and accelerate time-to-market.

The year ahead

Today's AI products pack together several compute die, fast I/O, networking interfaces, and multiple stacks of high-bandwidth memory. With so much silicon in one package, a single weak die can compromise the entire module. That's why test has spread to more points in the manufacturing flow — at the wafer, at singulated die, on the module, and increasingly at the board and system level. Known-good-die is really the best way to protect the investment that is being made in these advanced packaged products.

SHANNON POULIN

The second trend we're seeing is power. AI devices are now brushing past a kilowatt, many will be exceeding 2kW soon, and there are plans for >4kW products on the horizon. Entire racks can push toward the half-megawatt mark. Test systems must deliver that power while keeping devices safe, stable, and thermally controlled. As the industry shifts toward direct-to-chip liquid cooling, and begins to explore immersion, test equipment will need new ways to manage heat and replicate real-world operating conditions.

Lastly, new technologies like silicon photonics and co-packaged optics are pushing the capabilities of these new architectures. Bandwidth demands are rising so quickly that optics are moving closer to the compute die itself. In 2026, we'll see the early stages of real commercial deployment: small runs at first, but meaningful ones. This transition introduces new test needs that span both optical and electrical domains, from photonic wafer measurements to system-level optical checks once everything is assembled.

Across all of this, one theme stands out: test capability must scale as quickly as the devices it supports. Modular platforms that can be upgraded for new interfaces, higher power, or optical workflows will help keep AI programs on pace. In the year ahead, test will be an integral component in ensuring the quality and yield of devices that are exponentially more complex than anything we've seen before.

AI Looms Large as Test Applications Continue to Broaden

DOUG LEFEVER,
Representative Director and Group CEO, Advantest Corp.

The semiconductor industry is entering a new era in which complexity, cost, and performance pressures converge. Meeting these demands will require unprecedented collaboration across the supply chain. In 2026 and beyond, collaboration will be key to pioneering best-in-class test cells that drive velocity and innovation.

From a market perspective, we see artificial intelligence (AI) continuing to drive significant growth in the semiconductor market, spurring new innovations in advanced packaging, high-bandwidth memory (HBM), thermal control, and optical integration to support the next generation of high-performance GPUs. As these complex challenges combine, testing plays a key role in enabling customers to meet time-to-market and quality requirements.

DOUG LEFEVER

In the coming year, we anticipate continued advancements in 2.5D/3D packaging to enable higher performance in AI and high-performance computing (HPC) devices. Foundries and OSATs are making significant investments in next-generation packaging technology, such as chip-on-wafer-on-substrate (CoWoS), EMIB, through-silicon vias (TSVs), and co-packaged optics (CPO). HBM and other advanced memory technologies also rely on 3D stacking to offer the high processing speeds needed to fuel AI applications.

The increasingly complex architecture of 2.5D/3D chips presents various challenges during test. For example, heightened density and processing speeds elevate temperatures, increasing the risk of failure after wafer-level and final test. This necessitates specialized test equipment with sophisticated thermal-management capabilities and active thermal control. We foresee a growing need for more testing at the singulated-die level, where more precise thermal control can be achieved to capture failures before stacking and ensure only known-good die are packaged.

In addition to die-level test, customers are looking for more ways to reduce yield loss, especially as the cost of 3D packaged devices rises. In response, test companies are moving more test content to earlier insertions. For example, much of the speed and performance testing that used to be reserved for final test is now being performed at wafer sort or singulated die test to ensure that the die can perform high-performance workloads before they are packaged.

We are also beginning to see system-level test content being combined with other test insertions, ensuring better test coverage throughout the back-end flow. We expect all of these trends in test to continue into 2026 as customers seek ways to reduce yield loss and cut costs, and we look forward to seeing what the year ahead will bring.

How 2026 Policy Choices Shape the Semiconductor Landscape

ROYAL KASTENS, Vice President of Global Public Policy and Advocacy at SEMI

Geopolitical competition and evolving policy frameworks in 2026 will push the U.S. to sustain its technological leadership in semiconductor design, manufacturing, and innovation. The United States has led the global semiconductor industry with pioneering advancements in chip design, fabrication, and research, but rebuilding a robust domestic supply chain is a national security imperative and economic growth opportunity.

ROYAL KASTENS

For SEMI and our member companies in the global electronics value chain with U.S. operations, key policy areas for 2026 will include competitive trade policies, workforce development, long-term tax and R&D incentives, implementation of the CHIPS and Science Act, and pragmatic sustainability policies.

For the U.S. to meet its leadership goals in semiconductors, trade policies that preserve the supply chains essential to U.S. manufacturing and strengthen its industrial base are key. Simultaneously, a balanced export control framework secures U.S. innovation. A consistent, rules-based framework in alignment with allied nations will protect national security while sustaining U.S. semiconductor competitiveness globally.

To help continue to drive semiconductor investment in the U.S., tax incentives benefiting the entire supply chain will also be important in 2026. With key U.S. incentives approaching expiration while global subsidies are also increasing, the U.S. is in a pivotal period where pending decisions could shift the current landscape.

Another priority in 2026 is resilience to disruption—the shared responsibility of industry and government. Federal investment and private initiatives should be complementary and fill gaps where market incentives fall short. Resilience and industrial competitiveness also include environmental stewardship. This is why SEMI supports policies that enable continuous improvements while the U.S. seeks to advance its semiconductor manufacturing leadership.

Talent will remain critical to all aspects of the U.S. semiconductor industry's growth and competitiveness. In 2026, workforce needs will continue to influence both industry and government priorities and will be recurring topics as stakeholders assess how well current efforts align with long-term demand. Talent infrastructure, including training pathways and access to top tier talent, will continue to be essential in meeting industry needs.

The need to prioritize R&D also cuts across all key policy priorities. Every major policy area depends on a rigorous R&D pipeline, which Congress recognized in passing the CHIPS and Science Act that established key R&D incentives. Continued implementation of the CHIPS and Science Act and policies that support R&D strengthen every link along the semiconductor value chain.

The U.S. is at an inflection point on its technology leadership goals. The success of these policy priorities will help define whether the U.S. semiconductor ecosystem continues to grow stronger or risks fragmentation.

From Lab to Fab to Scale: Securing the Future of US Innovation

JESSICA GOMEZ, founder & CEO, Rogue Valley Microdevices

The semiconductor industry is navigating a period of profound transformation. While efficiency within global supply chains remains a core objective, today's market is increasingly defined by a shift toward domestic resilience and technological convergence. As we approach 2026, the strategic focus for U.S. manufacturers has evolved. Performance remains central, but it is increasingly limited by the complexities of multi-technology integration and the massive scaling requirements of the artificial intelligence era.

The surge in AI is driving an unprecedented demand for localized intelligence in edge devices, autonomous systems, and medical diagnostics. This shift is pushing the boundaries of MEMS, sensors, integrated photonics, and advanced packaging to their collective limits. To address these hyperscale requirements, the transition toward 300mm manufacturing has become a pivotal next step for the broader microelectronics ecosystem. Moving beyond the legacy 200mm standard provides the automation and film uniformity necessary for high-performance devices. Our own evolution from world-leading thin-film expertise in Medford, Oregon, to our new 300mm-capable facility in Palm Bay, Florida, reflects this industry-wide necessity for "lab-to-fab-to-scale" capability.

JESSICA GOMEZ

Geopolitical shifts and supply chain fragility have transformed semiconductors into critical strategic assets. For domestic foundries, the challenge is ensuring that innovators have a reliable path from prototype to high-volume production without leaving U.S. shores. This resilience is intrinsically linked to the combination of MEMS, advanced packaging, photonics, and logic dies. As traditional scaling reaches its physical limits, this convergence has become the new frontier for performance gains.

Leveraging high-density interconnects like through-silicon vias (TSVs) and redistribution layers (RDL) at a 300mm scale provides a unified domestic platform for vertical integration, allowing these diverse technologies to function as a single, high-performance system.

Supported by the CHIPS and Science Act, the expansion of U.S. manufacturing capacity is a pragmatic and bold response to a volatile global market. Establishing a robust 300mm ecosystem on the Space Coast ensures that the United States remains at the forefront of the technologies defining the next decade. We are excited to be part of this historic inflection point for American innovation as we build the necessary infrastructure to adapt and thrive in a rapidly changing world.

Europe's Semiconductor Opportunity: Meeting the Moment

STEPHEN M. ROTHROCK, Founder & CEO, ATREG, Inc.

The European Chips Act was meant to be a wake-up call. Three years later, the response has been underwhelming. Intel's German megafab is on hold, Wolfspeed's European expansion never materialized, and Broadcom pulled out of their $1 billion plan for an R&D site in Spain. The €43 billion initiative has produced a handful of meaningful commitments— ESMC, STMicroelectronics, Infineon, GlobalFoundries, and Silicon Box, but Europe's share of global chip production continues to slide.

STEPHEN M. ROTHROCK

Yet declaring Europe's semiconductor ambitions dead would be a mistake. The real opportunity is not about chasing Taiwan's leading-edge dominance or outspending America's subsidies. It lies in something Europe already does exceptionally well – specialty and mature-node manufacturing backed by world-class research infrastructure.

Consider the fundamentals. Europe's research ecosystem – imec, CEA-Leti, Fraunhofer, VTT – remains unmatched. As imec's Luc Van den hove has noted, "You can't make an advanced chip without European technology." The FAMES Pilot Line, one of five pilot initiatives within Europe and funded with €830 million, is bringing together these institutions to develop low-power technologies for automotive, IoT, and mobile applications. Critically, its *open access* policy gives European manufacturers early access to next-generation capabilities that competitors simply cannot replicate elsewhere.

Meanwhile, defense spending is surging. Germany has announced plans to double defense expenditure to €650 billion over five years. France, Italy, and the UK are following suit. This isn't abstract policy – it's real demand for mature-node chips in missiles, drones, and secure communications systems. Europe's reliance on Chinese legacy chip production for strategic applications has become untenable, demonstrated forcefully by the recent Nexperia situation.

Policymakers are taking notice. A European Chips Act 2.0 is already taking shape, with EU member states agreeing earlier this year to strengthen their collective position in semiconductors. Unlike the original legislation which offered no specific support for mature-node production, the next iteration is expected to target the legacy chips that underpin Europe's defense and industrial base. Importantly, European policymakers need to maintain the legacy semiconductor assets they already have and prevent them from falling into disrepair and closure. Whether for leading-edge 300mm applications or such specialty applications as photonics, numerous semiconductor firms globally have found creative solutions to refurbish mature fabs – ADI in Oregon, New Photonics in Belgium, and Octric Semiconductors in the UK are three examples worth replicating.

The strategic calculus is straightforward. Semiconductor companies without meaningful European capacity risk ceding ground to competitors who recognized this shift early. The window to establish presence ahead of the competition is open, but it won't remain so indefinitely.

EU Cybersecurity Regulatory Evolution and Its Impact on Semiconductor Manufacturing Equipment

DR. FAHAD GOLRA, Director of Product Innovation, Agileo Automation

European regulations on safety and cybersecurity are evolving and will affect industrial equipment, including semiconductor manufacturing tools, whenever they fall within scope. The Cyber Resilience Act (CRA), the Radio Equipment Directive (RED), and the new Machinery Regulation each focus on different aspects of digital, radio, and mechanical functionality. Together, they will influence how original equipment manufacturers (OEMs) design, certify, update, and maintain equipment over the next decade.

FAHAD GOLRA

The CRA establishes mandatory cybersecurity requirements for all products with digital elements. For semiconductor tools that include embedded controllers, communication interfaces, diagnostics, or remote update mechanisms, CRA obligations will apply starting in December 2027. Manufacturers must ensure secure planning, design, development, and maintenance, supported by vulnerability handling processes throughout the product lifecycle. They must also provide an SBOM (Software

Regulation	Primary Regulatory Focus	Practical Consequence for OEMs
Cyber Resilience Act (CRA)	Cybersecurity lifecycle of digital products	Formal cybersecurity lifecycle obligations, SBOM provision, vulnerability handling and update accountability across the product lifetime
Radio Equipment Directive (RED)	Product-level radio conformity and spectrum efficiency	Radio-specific conformity (spectrum use, EMC, antenna configuration); cybersecurity aspects progressively covered by CRA
Machinery Regulation	Safety of machinery, including protection against cyber-induced unsafe behavior	Safety assessment extended to digital control and cybersecurity threats that could impact safety, stronger change traceability, possible third-party assessment for high-risk configurations

Bill Of Materials), issue security updates in a timely manner, and maintain secure update mechanisms. The CRA also introduces reporting obligations starting in 2026. While the Act does not prescribe specific tools, OEMs will increasingly adopt software composition analysis and structured patch management to meet obligations regarding component visibility and vulnerability remediation. Products placed on the EU market must bear a CE marking, and national authorities will enforce compliance.

The RED applies to equipment that includes radio communication, such as Wi-Fi, Bluetooth, RFID, or 5G. While many semiconductor tools remain wired, the use of wireless diagnostics and sensors is increasing. The RED continues to govern radio performance, electromagnetic compatibility (EMC), and spectrum behavior. Meanwhile, the CRA will gradually take over cybersecurity obligations for digital products with radio capabilities, thus avoiding regulatory overlap.

The new Machinery Regulation modernizes safety requirements for machinery and now includes digital behaviors that influence hazardous motion or energy. For semiconductor tools that include robots, wafer handling systems, plasma modules, or high-voltage subsystems, any software or firmware affecting safety must be assessed. Manufacturers must demonstrate that updates, remote commands, or cyber incidents cannot create unsafe states. Depending on the nature of the safety functions, certain configurations may require a third-party assessment before the equipment can be placed on the EU market.

Although these horizontal regulations do not target semiconductors specifically, they will significantly impact semiconductor OEMs that integrate digital control, wireless functions, or machinery components into their equipment as early as next year.

Supply Chain Resilience is Key

ROSS BERNTSON, President & CEO, Indium Corporation

In today's 2026 geopolitical climate, a resilient global supply chain is no longer a competitive advantage—it's a necessity. At Indium Corporation, building and sustaining that resilience has been a deliberate, long-term effort rooted in partnership, diversification, and trust. As a materials supplier serving multiple industries, including the semiconductor sector—where reliability matters most—our approach to the global supply chain reflects who we are as a company: forward-looking and deeply committed to delivering for our customers.

ROSS BERNTSON

With manufacturing facilities around the world, our belief in producing materials close to our customers has consistently proven its value. This model allows for better service, faster response times, and improved inventory positioning, while helping to reduce exposure to price volatility. When required, we import materials that are not practical to produce locally, working closely with regional experts and authorities to actively monitor trends and market conditions. This balanced approach allows us to effectively align localization with the realities of a global supply network.

Looking ahead, this foundation allows Indium Corporation to continue prioritizing consistency in material standards at every facility as we maintain and grow our expanding portfolio of solders, fluxes, and advanced thermal interface solutions to meet evolving market demands. For example, across applications such as high-performance computing, AI, electric vehicles, and advanced packaging, one common requirement remains: advanced thermal solutions that ensure reliability, performance, and product lifespan. This is where our innovations in metal thermal interface materials come in to support new builds and future development to advance the technology. In parallel, we will introduce new members of our Durafuse® solder alloy technology family, addressing high-temperature lead-free requirements in power electronics as well as increasing demand for high reliability in low-temperature applications.

Guided by our motto,

"From One Engineer to Another®," industry partnership continues to play a key role in our success. In Taiwan, for example, we're especially excited to introduce new materials that were co-developed with in-country partners. Collaborating directly with manufacturers in one of the world's most influential semiconductor ecosystems provides invaluable insight into emerging needs and what's coming next in semiconductor materials.

As we move through 2026, we will further strengthen our team's focus on close collaboration with customers, aligning supply strategies with product roadmaps to keep pace with their ever-evolving innovations.

Market Growth and Federal Incentives Power Semiconductor Construction

JEFF PAYNE, Vice President and Account Manager, Skanska Advanced Technology

JEFF PAYNE

The semiconductor market in the USA is experiencing strong momentum, driven by rapid technological advancements, rising demand for smart devices and the accelerating shift toward AI-powered applications, according to Statista. This growth is reshaping the industry landscape and fueling significant investment.

The Semiconductor Industry Association (SIA) reports that landmark government incentives and research funding have catalyzed a wave of private-sector investment. Companies have committed more than $500 billion to revitalize the domestic chip ecosystem, setting the stage for a projected tripling of US chipmaking capacity by 2032. Industry analysts expect these developments to generate more than 500,000 jobs nationwide, including 68,000 facility roles, 122,000 construction jobs and more than 320,000 additional positions across the broader economy in the coming years.

In July 2025, the USA enacted legislation that strengthens a critical tax incentive, the Advanced Manufacturing Investment Credit (AMIC), which encourages investment in semiconductors. The new law increases the AMIC rate with credit that may be extended beyond its 2026 expiration and expanded to cover chip research and design (SIA).

Government policies like these are catalyzing new private-sector partnerships and large-scale capital investment, prompting leading semiconductor and technology companies to collaborate on domestic manufacturing, research and supply-chain expansion initiatives.

Meanwhile, current US policies encourage onshoring of manufacturing and technology, driving significant financial commitments from major companies for construction projects. Given these factors, it's clear that the US semiconductor sector is primed for substantial growth.

To meet the high-technology sector's increasing growth, Skanska established a specialized unit, Skanska Advanced Technology (SAT). With semiconductor experience dating back to the 1990s and more than 240 facilities completed or under construction, this group of 180+ construction experts across the country delivers complex, large-scale projects. SAT is well positioned to respond as funding for the 300mm semiconductor sector advances.

It's Time to Reduce Costs & Timelines for US Fab Construction

ALLAN FULLER, President, Foresight Technologies

Looking ahead to 2026, a shortage of skilled labor and established sub-fab equipment supply chains will continue to drive up construction costs and delay completion of US semiconductor fabrication facilities. Although it might seem cheaper and faster in theory, overseas IDMs can't efficiently bring their home-grown supply chains and trained staff to build US fabs. A single delay in the installation of foreign equipment can add days, weeks, or even months to the construction timeline. This skill and capability gap will grow as fabs expand into more rural, non-traditional areas. Until that regional ecosystem matures, this cycle will repeat at each construction site.

ALLAN FULLER

Addressing these issues will require IDMs, construction contractors, and foreign equipment suppliers to develop domestic solutions that improve process performance, reduce logistical friction and lead time, and do so at a lower cost. This is best accomplished by partnering with US suppliers to localize their design and manufacturing. It will also increase design flexibility, enabling quick corrections, schedule recovery, or future unplanned upgrades. A long-term vision involves standardized modular designs that can be prefabricated off-site to enhance quality, decrease on-site labor, and lower build and expansion costs.

These changes build a more resilient and efficient supply chain for a relatively young industry currently experiencing rapid growth. It's a straightforward calculation: the current approach is not economically sustainable, so every stakeholder in their sector must develop innovative solutions and adopt new processes to keep semiconductor fabs cost-effective and on schedule.

Foresight On-Site was established to help create a US cost advantage. With over 400 US employees and 30 years of experience in high-purity system fabrication, we aim to provide domestic high-volume manufacturing along with

licensed pipefitting services to support base-build construction, equipment installation, and tool hookup.

Advanced Packaging: The Top Enabler

BOB PATTI, Founder and CEO, NHanced Semiconductors

In 2026, I expect advanced packaging to continue its growth as the industry's top enabler. More-than-Moore is the future and advanced packaging is key. Three areas of advanced packaging where I foresee major advances are die-to-wafer hybrid bonding, photonics, and interposers.

BOB PATTI

Die-to-wafer hybrid bonding

New technologies allow high speed die-to-wafer hybrid bonding with ultra accurate overlay, thereby reducing cost and increasing throughput, erasing the advantages previously held by wafer-to-wafer bonding. We have also seen steady improvement in known good die (KGD) approaches. Together, these two advancements have pushed component manufacturers to create their own chiplets for next generation devices. Bonded interconnect is 100x denser and 100x lower power than soldered connections. Die level hybrid bonding has not yet gone mainstream, but the path seems clear: 2026 will see further chiplet enablement and large scale prototyping to prove that hybrid bonding is ready. By 2028-2030, I predict high volume manufacturing of hybrid bonded chiplets.

Photonics

Photonics continues its steady progress toward usage both in-package and package-to-package. Optical EIC and PIC integration and laser attachment are already commonplace; however, fiber attachment is still labor-intensive and relatively low volume. Optical interconnect is the obvious solution for the ravenous bandwidth needs of AI and HPC, but there is no high-volume manufacturing method for adding a thousand fibers to a module. The key breakthrough required is silicon level connectorization of optical interconnect. Solutions are already being tested and might debut in the coming year. When ready, new connectors will trigger rapid evolution in machine architectures and data centers.

The next "coming of age" for photonics will be high density optical circuits to support the new, massively parallel optical interconnects. Fueled by silicon photonics advancements and intimate incorporation of new materials like GaN and TFLN, commercial products with true ≤1 pJ/bit are at hand. First commercial shipments may take place in 2026.

Interposers

Interposer size has been limited to 3.3 reticles by the CTE mismatch between silicon interposers and the organic substrates they are assembled on. Nonetheless, we see increasing demand for larger interposers. Glass interposers, with their higher CTE, are poised for a market breakthrough to fill this need. Glass interposers with sizes greater than 10 full reticles are coming – perhaps as early as 2026.

Building Differentiated Advanced Packaging Solutions and Scaling Chiplet Production

JIM STRAUS, VP of Sales, ACM Research

As the semiconductor industry enters 2026, a strong transition is anticipated, with advanced packaging firmly established as a critical engine of innovation. Artificial intelligence (AI) and high-bandwidth memory (HBM) workloads will continue to drive device sizes, interconnect density, and power budgets, forcing an accelerated shift from traditional wafer-based processes toward glass substrates and 3D stacking. Throughout this transition, chiplets will remain a central focus. However, the industry's focus will also broaden from what we integrate to how and where we build devices, with wafer-level packaging (WLP) and panel-level packaging (PLP) both playing crucial roles.

WLP is expected to continue growing as the production standard for 3D integration, headlined by its use in AI and HBM devices on 300mm wafers using silicon interposers. At the same time, PLP is emerging as the next lever for cost reduction and capacity expansion. According to Yole's 2025 PLP report, the PLP market is projected to reach $600 million by 2030, with a CAGR of 27% from 2024 to 2030. This growth is primarily driven by its cost advantages and higher area utilization, simultaneously meeting the technical requirements of both advanced and traditional packaging.

JIM STRAUS

By delivering significant cost savings and achieving substrate utilization beyond 80%, high-end fan-out panel-level packages (FOPLP) and 2.5D interposer technologies are projected to drive AI, HPC, mobile, and high-end consumer markets. Enabled by equipment innovations, the evolution from round wafers to square glass panels will also allow for more dies per substrate, higher throughput, and better economics for increasingly complex packages. Increasing investments from equipment and material suppliers will go toward building a comprehensive ecosystem that meets customer needs.

For all its benefits, this transition will not come without challenges. As panel sizes adapt from roughly 310 x 310mm to 600 x 600mm and beyond, a lack of standardization is expected to raise both R&D and capital costs for OSATs, fabs, and equipment vendors. Developing

tools that can flexibly handle various glass panel sizes while maintaining uniform process performance and integration into evolving production flows will be a priority in 2026.

At ACM Research, our focus remains on partnering closely with our customers to commercialize differentiated packaging solutions, helping move PLP from pilot lines into mainstream manufacturing. We continue to collaborate with device makers to deliver advanced packaging technologies that support the industry's transition from wafer to panel.

Building the Workforce the Moment Demands

SHARI LISS, Vice President of Global Workforce Development and Initiatives, SEMI

Talent is now core infrastructure

As we look ahead to 2026, I'm increasingly optimistic about where the semiconductor workforce is headed, not because the challenge has eased, but because the world is seeing talent in this industry as the strategic priority it has always deserved and needed to be.

The scale of investment flowing into semiconductor manufacturing, advanced packaging, and research is unprecedented. What's encouraging is that workforce development is now part of that conversation from the start. More leaders across industry, government, and academia recognize that talent is not a downstream issue, it is core infrastructure for innovation, economic competitiveness, and national security.

SHARI LISS

From policy to practice

Over the past few years, policy commitments have laid out important groundwork. In 2026, we'll see more of that policy translated into action on the ground. Federal priorities are increasingly aligned with state strategies and employer needs, giving education and training providers the clarity and confidence to modernize programs, emphasize hands-on learning, and prepare individuals for real roles, not just credentials. That alignment matters, because speed and relevance are everything in a fast-moving industry.

Expanding pathways, strengthening retention

I'm also encouraged by how quickly the industry is embracing more flexible pathways into semiconductor careers. Four-year degrees remain important, but they're no longer the only on-ramp. Apprenticeships, short-term training, certifications, and earn-and-learn models are proving that we can expand access, reduce time-to-hire, and improve retention at the same time. These pathways are opening doors for veterans, career changers, and students who might otherwise never see themselves in this industry.

Making opportunity visible

Technology will continue to play a growing role in workforce development as well. In 2026, digital tools that connect career exploration, skills validation, training options, and live job opportunities will become essential to how talent moves through the ecosystem. When individuals can clearly see how their skills translate to opportunity, and employers can more easily identify readiness, the entire system works better.

Investing earlier, collaborating better

Finally, I'm optimistic because the industry is investing earlier, sparking curiosity, building awareness, and connecting learning to real-world impact long before career decisions are made.

The workforce challenge remains urgent. But in 2026, we're no longer asking whether we can solve it; we're focused on how quickly and how well we do on a global scale.

Workforce Development Challenges

CHRIS HENDERSTON, President, Semitracks

CHRIS HENDERSON

At the start of 2025, there was a lot of excitement around workforce development. This excitement decreased markedly following the US Commerce Department's decision to stop activities through Natcast. Although Natcast is now basically defunct, the National Network for Microelectronics Education (NNME), through the National Science Foundation and the SEMI Foundation appears to still be moving forward. In the long term, it still remains to be seen how effective these training programs will be, especially given the fact that several of the larger employers of these potential employees have delayed or mothballed expansion plans, as we predicted would happen. The economy in 2025 held up reasonably well, and will likely hold up through 2026, since this is an election year in the United States, and the party in power will want to see the economy doing well leading into the elections. The main negative factor is the employment outlook. A number of firms have conducted mass layoffs in recent months, and this could weigh on consumer spending. It is also not clear how much longer the AI-fueled boom in segments of the semiconductor market will last, given the concerns about debt levels and "circular financing" agreements between many of the major players. We still believe there is a longer-term trend in place to "reshore" some manufacturing, and this should create an environment where the industry should be able to

absorb new workers in 2026. More flexibility in training the workforce is still needed to address the vagaries of the market and the industry's response to it. Semitracks, Inc. is positioned to help with this training need. We can scale our training as needed and provide customized solutions for key gaps in talent and workforce personnel. 2026 should again be an interesting year, given the uncertain demand in the electronics industry, so creative solutions may be necessary for workforce development. We stand ready to help.

Materials 2026 Forecast Trends

L. SHON-ROY, President, Materials Analysis, Techcet by Techinsights

L. SHON-ROY

2026 Forecast outlook from Techcet's materials experts on what they expect to see in the coming year in terms of critical technology and business trends relating to materials:

Business Trends

- The materials market is expected to improve in 2026, growing 7% to 8% over 2025, driven by increased demand for materials from chip expansions and continued growth of AI applications.
- Geopolitics and trade wars will continue to drive up prices in metals and minerals, many of which originate from China. Key examples include tungsten, rare earths, gallium, germanium, etc.
- The US supply chain continues to expand, adding manufacturing capacity for materials to support chip expansion plans. This trend is driving investment from Asian companies seeking a footprint in the US as well as US-headquartered materials companies.
- Large MNEs that have electronic materials business units continue to re-evaluate their involvement in the semiconductor industry. Splitting off their electronics BU insulates the rest of their company from the cyclical nature of the semiconductor industry and provides an easier path to divestment.

Technology Trends

- ALD/CVD precursors and CMP materials are still the big winners in materials growth rates for the coming years due to increasing demand for 3DNAND, advanced logic, and advanced DRAM. AI has boosted demand for these materials needed for HBM.
- PFAS-free materials are of high interest but are coming into the market slowly. Slowness is attributed to the low cost and plentiful availability of traditional PFAS-containing materials from China, as well as to the easing of US environmental regulations.
- Technical challenges and opportunities exist for cleaning chemistries and low-emission etch chemistries needed for advanced devices in the sub 5nm area and advanced memory devices.

Supply Chain

- Increased Geopolitics, trade wars, tariffs, and embargoes drive ongoing concerns about the availability of raw materials, especially metals and minerals from China. Current Chokepoints include:
  - Metals used in chip production that are highly dependent on China and subject to export permit restrictions include: tungsten, copper, gallium, germanium, and rare earths.
  - Fluorocarbons - Europe and the US lack sufficient capacity to support CF gas semiconductor industry demand, while China has ample capacity.
  - T-Glass and advanced packaging substrates are in short supply due to high demand for AI chips - expected to continue until mid 2026.
- China has a lower hurdle rate and easier pathway to overcome the 3-key challenges that must be addressed to develop new raw materials sources: 1) Permitting & Environmental Regulations, 2) Plant build timing & resources, and 3) Technical know-how:
  - Permitting & Environmental Regulations required for new mining or chemical processing plants are challenging to overcome in the US and Europe because of strict onsite review and community involvement - often requiring 2-3 years to get through, versus parts of Asia, i.e., China (< 1year).
  - Building a mine and/or process plant to refine the ore takes time to source the needed equipment and personnel once the site is identified. The time required for this step: 1-3 years.
  - Technical know-how of metal/mineral refining is lacking in the west where processes must be developed that are friendly to humans and the environment.

Edge AI and Embedded Processing Innovation Will Usher in a New Era of Physical AI

RON AMICHAI, SVP & GM, Embedded Processing & DLP® Products, Texas Instruments

RON AMICHAI

In 2026, advancements in edge AI technology and embedded processing will converge to usher in the era of physical AI. By moving AI out of the cloud and into the physical world, the next generation of intelligent, efficient systems will be smarter, safer, and more responsive. With improved power efficiency and on-chip intelligence, intelligent devices will become the standard to sense, interpret and act in real-time. SD

SEMICONDUCTOR DIGEST

NEWS AND INDUSTRY TRENDS

Years of Progress