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TrueMask® ILT MWCO: Full-Chip Curvilinear ILT in a Day, and Full Mask Multi-Beam and VSB Writing in 12 Hours for 193i

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ABSTRACT

Since its introduction more than a decade ago, inverse lithography technology (ILT) has been seen as a promising solution to many of the challenges of advanced-node lithography. Numerous studies have demonstrated that curvilinear ILT mask shapes produce the best process window. However, the runtimes associated with this computational technique have limited its practical application. In 2019, D2S introduced an entirely new, stitchless approach for ILT [20]. This system includes a unique GPU-accelerated approach that emulates a single, giant GPU/CPU pair that can compute an entire full-chip ILT solution at once. This novel approach, systematically designed for ILT and GPU acceleration, makes full-chip ILT a practical reality in production for the first time. The masks used to validate wafer results for this system were written by a multi-beam mask writer.

The question remained of whether it was possible to use this new approach to ILT in a way that could be written by a variable-shaped beam (VSB) mask writer. This paper introduces a new method, in which a process called mask-wafer co-optimization (MWCO) is performed during ILT optimization. This new approach enables curvilinear ILT for 193i masks to be written on VSB mask writers within reasonable write times. It shortens the total turnaround time so that VSB mask writers can produce full-chip, curvilinear ILT masks within a practical, 12-hour time frame, while also producing the largest process windows. It should be noted that this enables curvilinear or any-angle targets for the wafer design to be processed by curvilinear ILT and then written by VSB mask writers for 193i processes. While MWCO as a concept can be used for multi-beam mask writers as well, this paper is focused on MWCO for VSB mask writers.

Keywords: Photomask, GPU, Inverse Lithography Technology, ILT, Curvilinear ILT, Mask Wafer Co-Optimization (MWCO), Multi-beam Mask Writer, VSB Mask Writer, MDP, MPC

1. INTRODUCTION

1.1 Full-Chip, Curvilinear ILT is Now a Practical Reality

Inverse lithography technology (ILT) – a mathematically rigorous inverse approach that determines the mask shapes that will produce the desired on-wafer results – has been seen as a promising solution to many of the challenges of advanced-node lithography, whether optical or EUV. Since its introduction more than a decade ago [1-17], there have been numerous studies that demonstrate that curvilinear ILT mask shapes, in particular, produce the best process windows [18]. However, until recently, the runtimes associated with this computational technique have limited its practical application to critical "hotspots" on chips [19]. The solution to the runtime problem for ILT has been particularly vexing, as the traditional approach to runtime improvement – partitioning and stitching – has failed to produce satisfactory results, either in terms of runtime or in terms of quality. At the 2019 SPIE Photomask Technology Conference [20], we detailed an entirely new, stitchless approach, creating a purpose-built system for ILT, called TrueMask® ILT. This system includes a unique GPU-accelerated approach that emulates a single, giant GPU/CPU pair that can compute an entire full-chip ILT solution at once, in a single day. This novel approach, systematically designed for ILT and GPU acceleration, made full-chip ILT a practical reality in production for the first time.

The 2019 paper details how TrueMask ILT meets all of the requirements for a production-ready full-chip, curvilinear ILT solution: it integrates curvilinear mask rules to produce mask-rule-checking (MRC)-clean results; it meets edge-placement error (EPE) requirements; its results are continuous and symmetric; it demonstrates both on-grid and off-grid invariance; it is symmetric from any angle (Figure 1).

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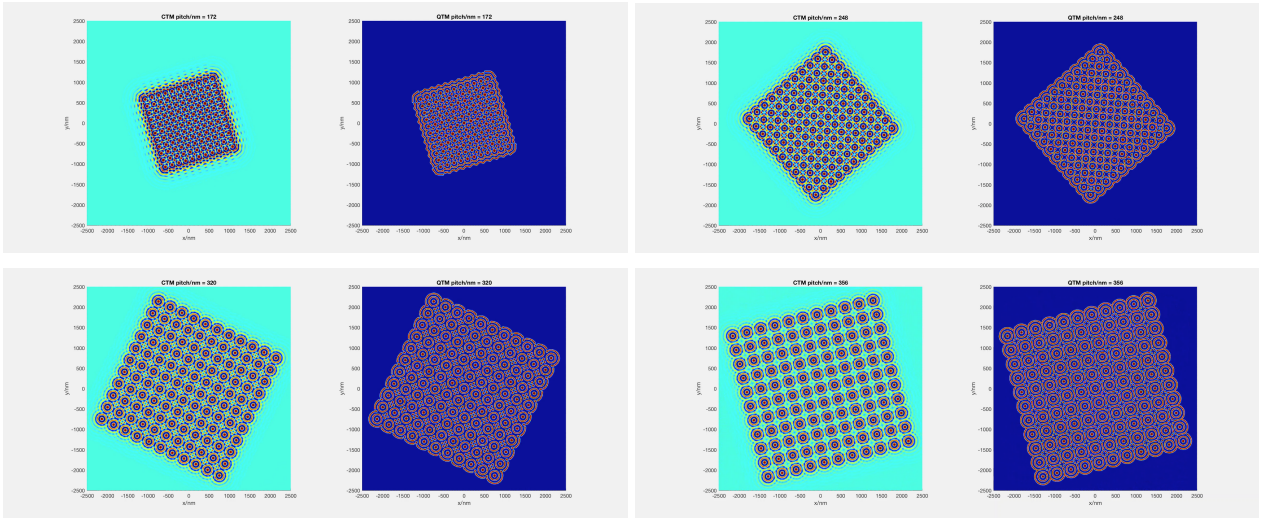


Figure 1: Continuous Tone Mask (CTM) and Final ILT mask for an equal-pitch contact array at on-grid and off-grid situation, pitch change, plus rotation demonstrating TrueMask ILT solutions are symmetric and rotation invariant [20]

To validate TrueMask ILT results, D2S worked with Micron Technology to write masks and print wafers using the Micron Technology process of record (POR) [20, 21]. The ultimate goal for curvilinear ILT is to achieve the best process window, so in this evaluation, process windows were compared between OPC and TrueMask ILT using the Micron POR. Critical dimensions (CDs) were measured to quantify the size of the process window between OPC and TrueMask ILT.

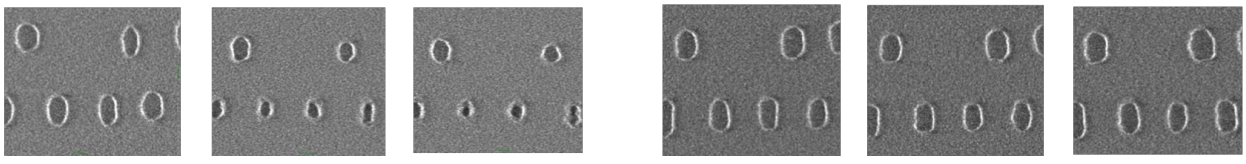
Figure 2 shows the wafer-print matrix result for a random contact layer. Unlike with Figure 1, these are all cases where the contacts are arranged in a Manhattan layout, without introducing non-orthogonal configurations. The target CD was 62.8nm; all dies with CD within a 10% variation are considered to be within the required process window. The CD measurements that meet the conditions within the process window are highlighted in green in the chart. Notice that the x axis is the focus, y axis is the dose (to be consistent with the process window plot). Three wafer images at the process center and two process corners are also shown below the charts. Compared to the Micron POR OPC, TrueMask ILT enlarged the process window by over 100%.

OPC Process Window

	Dose (mJ)	Defocus (nm) -60	-40	-20	0	20	40	60	Dose(%)
Latitude	21	55.4	59.6	62.5	61.2	60.5	51.6	41.8	93.3%
	21.5	56.3	57.3	63.7	61.0	58.1	52.9	40.3	95.6%
	22	57.3	60.8	61.0	60.8	57.1	48.3	41.6	97.8%
	22.5	54.0	52.8	60.1	55.8	54.7	52.1	39.3	100.0%
	23	49.4	54.4	55.3	60.3	54.5	49.2	36.1	102.2%
	23.5	49.2	50.9	54.5	55.0	51.6	46.1	33.9	104.4%
	24	54.0	56.2	54.8	49.9	50.9	44.7	28.6	106.7%

TrueMask ILT Process Window

	Dose (mJ)	Defocus (nm) -60	-40	-20	0	20	40	60	Dose(%)
Latitude	21	57.7	60.5	59.6	64.1	58.8	62.1	58.4	93.3%
	21.5	54.0	56.9	58.1	60.9	59.0	62.8	59.4	95.6%
	22	60.6	55.4	59.3	60.3	57.9	59.5	58.8	97.8%
	22.5	54.5	57.7	57.6	60.6	56.2	59.4	57.9	100.0%
	23	52.0	56.5	57.0	56.2	57.3	60.9	58.3	102.2%
	23.5	52.2	56.7	55.1	54.6	54.9	55.6	54.7	104.4%
	24	48.6	52.7	51.6	50.8	56.1	52.3	56.1	106.7%



Best Focus Norm Dose | 60nm Defocus Norm Dose | 60nm Defocus 93.33% Dose

Best Focus Norm Dose | 60nm Defocus Norm Dose | 60nm Defocus 93.33% Dose

Figure 2: Process window CD measurements for standard OPC vs. TrueMask ILT of Micron Technology's POR. The green regions are within process window. TrueMask ILT increases the process window by more than 100% [20].

1.2 Could This Full-Chip ILT Approach Be Extended to VSB Mask Writing?

The approach detailed in the 2019 paper relied on multi-beam mask writing, an important new development in mask writing that is pixel-based, rather than shape-based, and so is shape-agnostic in terms of write-time. The question that remained was if the benefits of full-chip, curvilinear ILT could be extended to the masks created by variable-shaped beam (VSB) mask writers that make up the majority of equipment in the mask-shops around the world today. In this paper, we will detail a mask-wafer co-optimization (MWCO) method that combines with established techniques, such as overlapping shots and mask and wafer simulation, to create Manhattanized, full-chip, curvilinear ILT mask shapes that VSB mask writers can write within 12 hours.

EUV does not need curvilinear ILT today. Because of the smaller mask features sizes of EUV masks, and because that in turn requires slower resists to be used for EUV masks, multi-beam mask writers are needed for EUV masks. But for 193i processing, advanced nodes need as much edge-placement accuracy as possible. The improved process windows that are possible from curvilinear ILT can help greatly. This is why it is important to enable curvilinear ILT for 193i to be written on widely available VSB mask writers.

2. MASK-WAFER CO-OPTIMIZATION FOR FULL-CHIP CURVILINEAR ILT FOR VSB MASK WRITERS

2.1 Mask Data Preparation and Mask Process Correction for Curvilinear ILT Masks

The conventional approach to Manhattanizing curvilinear ILT masks requires a trade-off of accuracy for ILT runtime and the write time on the VSB mask writer. It is possible to get very close to a curvilinear target using many small rectilinear mask shapes to form curves with small "jogs" or "stair-steps." This approach creates fairly good curvilinear mask shapes using VSB writers. However, the shot count involved in this approach leads to impractical write-times if it were to be used on a full-chip ILT design. Alternatively, jog and step-sizes can be made larger, say 20nm, to contain VSB shot count, but even then, if practiced at a full-chip scale, write times would be prohibitive using conventional fracturing (without overlapping shots). Combined with the long runtimes of the traditional ILT software, even when running on a large bank of CPUs, ILT has been confined to "hotspot" use only. Yet the need to run ILT for hotspots suggests that there is general understanding that ILT produces superior process windows for the wafer.

2.2 Overlapping Shots and Simulation Enable Full-Chip, Curvilinear ILT Using VSB Mask Writers

Overlapping shots is a technique to reduce shots and improve dose margin for angled lines and curvilinear features to be written by VSB mask writers [22, 23]. Figure 3 shows a typical curvilinear ILT mask pattern, fractured for a VSB mask writer. The pattern on the left uses conventional MDP for VSB; the pattern on the right, employs MDP with overlapping shots to create the same pattern. There are two observations from this example: first, overlapping shots can significantly reduce total shot count; and second, the majority of shots in this case (and in most production designs) are for the sub-resolution assist features (SRAFs) – which do not print – not for the main features. As we know, SRAFs have far less impact on the wafer edge-placement error (EPE) as compared to main features. For any given target main feature in a contact layer, an overwhelming number of shots are used for the SRAFs in a conventionally fractured solution. Overlapping shots produce SRAFs that perform well without devoting so much of the VSB write-time to producing them.

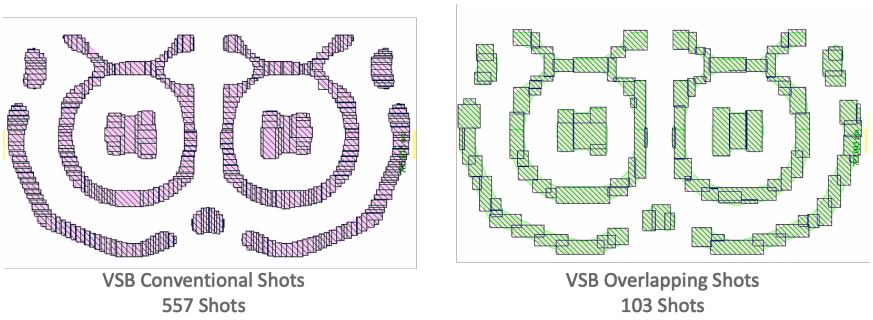


Figure 3: Example of a curvilinear ILT mask pattern written by VSB mask writer with conventional (fracturing) shots and overlapping shots.

2.3 Mask Wafer Co-Optimization (MWCO) Is the Key

Today's semiconductor manufacturing process separates the responsibilities between the OPC/ILT shop and the mask shop. The OPC/ILT shop has the responsibility to specify the desired mask shapes in order to achieve the best wafer results; the mask shop has the responsibility to manufacture the masks as close as possible to the shapes specified by OPC/ILT. Realistic limitations of mask making are codified as mask design rules that the OPC/ILT shop needs to obey when specifying mask shapes. Other realities of mask making are considered in OPC/ILT as well, most notably the consideration that VSB mask writing that is best for Manhattan (axis-parallel) rectangles with some provisions for 45-degree triangles. Since a major factor in mask cost and mask yield is mask write time, and the principle factor in mask write times (given a speed of resist dictated by the mask process for VSB-based mask writing) is the shot count, OPC/ILT tries to minimize mask shot count by various techniques, such as matching jog locations on opposite sides of a line [24]. With ILT, a Manhattanization process is explicitly invoked wherein the wafer shape is optimized given a certain minimum jog size, such as 20nm (mask dimensions) to avoid creating shapes that would take too many shots in the VSB writer [25]. But whether complex OPC or ILT, the specified mask shapes are complex, mostly rectilinear shapes with small 90-degree jogs, often with jog lengths of 20nm(mask) or less. Manufactured with mask processes that have a blur radius of 20-25nm (mask), these jogs are understood to become curves on the mask, often with the adjacent jogs interacting with each other. There is always a difference between the specified rectilinear shapes and the actual, curvilinear mask contours that result from that specification. Overlapping shots take advantage of this difference, using it as a tolerance in edge placement of the mask contour that can reduce shot count, while still shooting approximately the same contour, within the original EPE that the actual mask shape was going to have anyway.

In this separation of responsibilities, determining overlapping shots that could write the specified mask shapes was the domain of mask making. Even if error tolerances are within the original expectations, the idea that the originally specified shape is being slightly modified is disconcerting to the mask shop. Simulation-based contour checking is required, for example, because XOR checks will not pass.

MWCO marries curvilinear ILT with curvilinear MDP for VSB writers using overlapping shots. MWCO incorporates overlapping shot generation and mask-wafer double simulation into the ILT process, so that the output of the OPC shop is already optimized for shot count. By using double simulation, wafer EPE is iteratively optimized while manipulating VSB shot edges to produce rectilinear target mask shapes that are known to be writable on a VSB writer, with a known and an acceptable shot count.

This paper will demonstrate the method and its results.

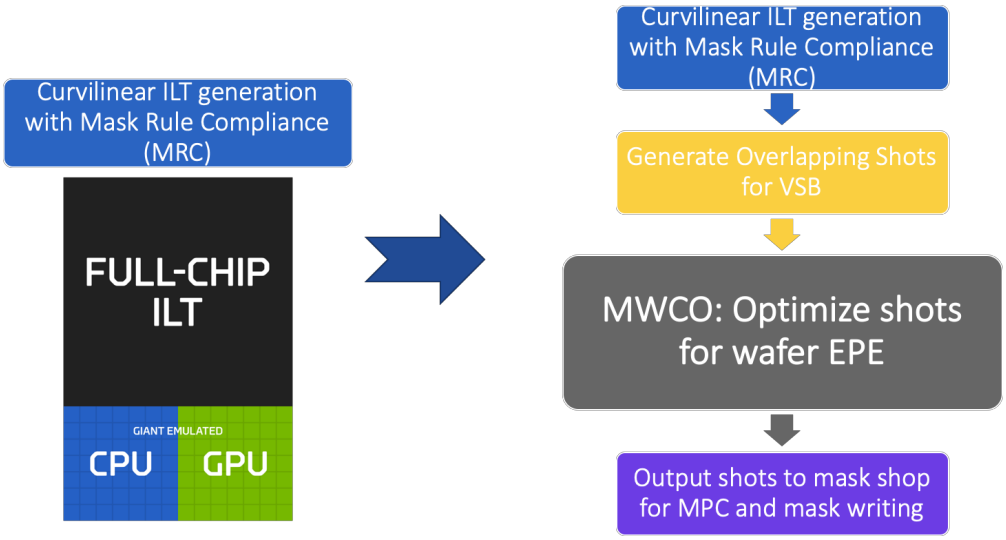


Figure 4: MWCO flow for full-chip, curvilinear ILT for VSB mask writers

2.4 Small Jogs on Mask Filtered by Band-limited 193i Scanner - Use Bigger Shots & Simulation to Reduce Shot Count

There are a number of observations that are leveraged in MWCO. The first observation is in regard to the jogs created when small rectilinear shapes are used to create larger, curvilinear shapes: Since the scanner is a band-limited optical system, small jogs on mask are high frequency and will be filtered out by scanner optics. Particularly with 193i, the effect is large and makes a significant difference in required shot count for VSB. As shown in Figure 5, when the jog size is increased from 170nm to 200 nm to 226nm, there is no impact on the wafer EPE – the wafer EPE for each of these jog sizes is zero. When the jog size is increased to 254nm, the wafer EPE is not zero, but is still less than 1nm, and no modulation in the wafer shape is observed. When the jog is even larger, for example, 310nm, then modulation is observed in the wafer shape, and the wafer EPE is larger than 1nm. This means we have some degree of freedom to move small jogs, and we also can use bigger shots with mask-wafer simulation to reduce shot count.

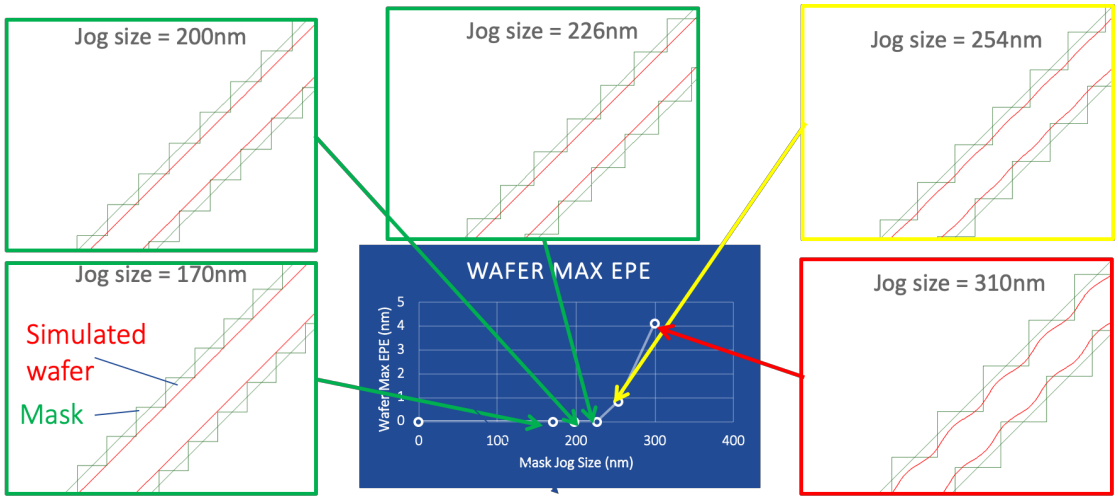


Figure 5: Mask jog size and its impact on wafer shape and wafer EPE

2.5 Overlapping Shots + Mask-Wafer Simulation = Fewer Shots for the Same Wafer EPE

The second observation is that for the same wafer EPE, many fewer shots are needed when overlapping shots are used. As shown in Figure 6, for the same 200nm jog size, and wafer EPE 0nm, overlapping shots can reduce the shot count of a diagonal line by nearly half.

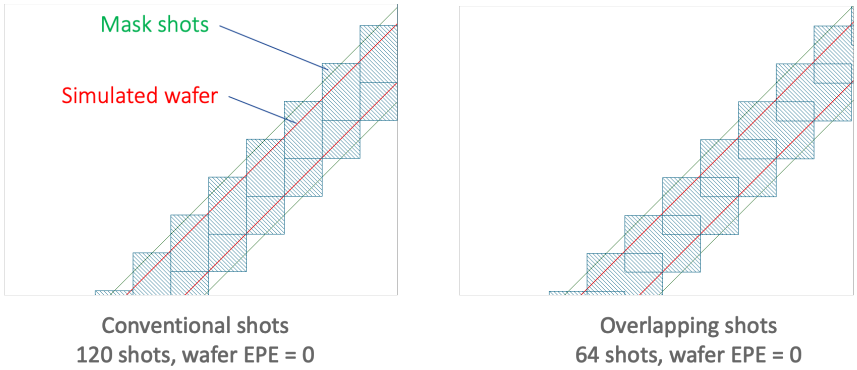


Figure 6: Conventional shots and overlapping shots to print the same angled line on wafer, using conventional shots (left) and overlapping shots (right).

2.6 Balance Shots for Write Time and Mask-Pattern Fidelity; Main Features: Conventional, SRAFs: Overlapping

The third observation is that majority of the shot count for any given mask is from curvilinear SRAFs. Because SRAFs have relatively little impact on wafer EPE, overlapping shots can be used on SRAFs to dramatically reduce shot count. Main features, on the other hand, have a large impact on wafer EPE; therefore, conventional shots can be used, as shown in Figure 7.

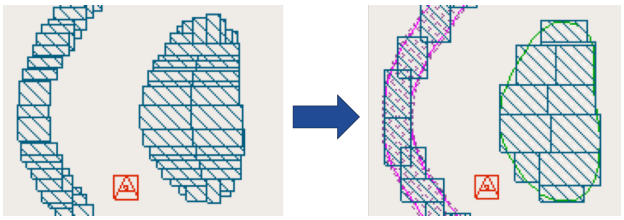


Figure 7: Illustration of writing SRAFs with overlapping shots, while writing main features with conventional shots

2.7 MWCO: The Key is to Minimize and Move Shots based on Wafer EPE, not Mask EPE

Figure 8 shows an example contact array with curvilinear ILT producing desired curvilinear mask target shapes, then VSB shots being generated for it using overlapping shots as previously published [22, 23, 26]. In the figure, green lines show the wafer target, red lines show the wafer image simulated from mask images simulated from the VSB shots in a double simulation process. The VSB shots are shown as hatched blue rectangles. Overlapping shots are shooting SRAFs on the mask that do not print on the wafer. For the SRAFs, thin brown lines reflect the target curvilinear mask shapes output by curvilinear ILT. Non-overlapping shots shoot the main features, but with shot count just large enough to produce the target mask contour as specified by curvilinear ILT (not shown). MDP for overlapping shots is simulation-based, with iterative optimization to produce a shot configuration that produces the desired mask contour while maintaining a low shot count, taking advantage of the natural corner-rounding in the mask process, which is especially prominent with SRAF dimensions. To the right is a zoomed-in picture of the two main features on the lower right of the contact array. Without using MWCO, the red contour of the simulated wafer image comes within 2nm EPE after mask-wafer double simulation. Because this process first produces the target curvilinear mask shapes using curvilinear ILT, and then separately optimizes the VSB shots to hit the desired mask contours, the trade-off with shot count inevitably results in accuracy loss, such as this 2nm EPE.

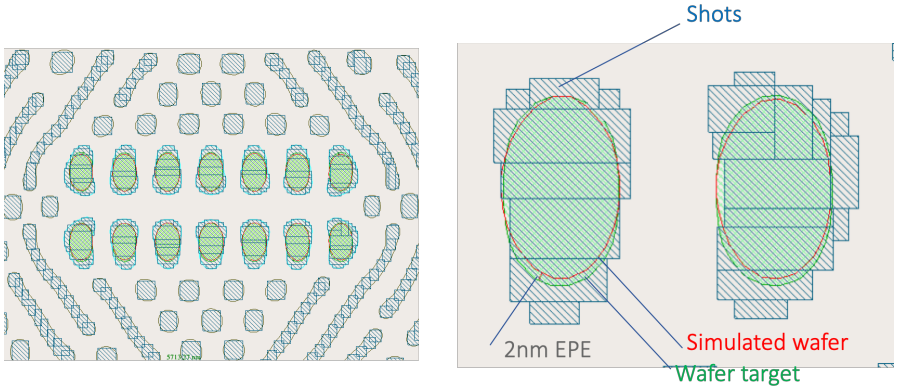


Figure 8: VSB shots generated to minimize mask EPE

The wafer results can be much improved with MWCO. Figure 9 shows the results when the shots to produce the mask contours are moved based on mask-wafer double-simulated *wafer* EPE. By taking this approach, without changing the shot count or shot configuration much, the wafer EPE is reduced from 2nm to 0nm at the same location and less than 1nm in all the shapes. Iteratively optimizing VSB shot edges while optimizing for *wafer* EPE significantly improves the ability to target curvilinear mask shapes while minimizing impact on shot count.

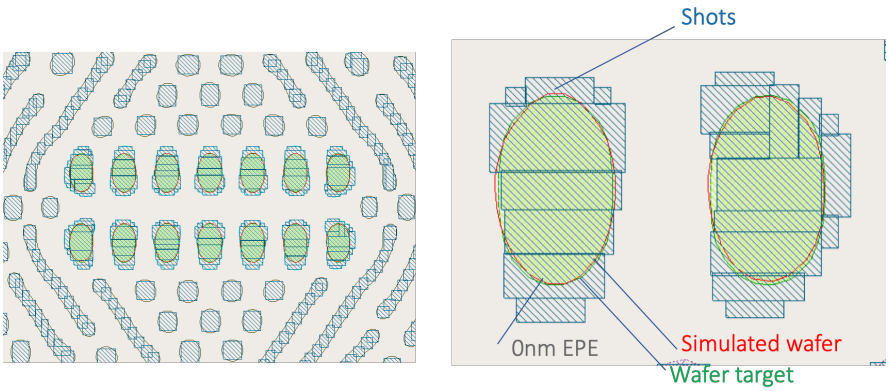


Figure 9: VSB shots generated to minimize wafer EPE

3. VSB MASK WRITER RESULTS FOR FULL-CHIP, CURVILINEAR ILT USING MWCO

3.1 Shot Density is the Key to Practical Write Times for VSB Mask Writers

Previous works have shown that a multi-beam mask writer [27] can write a full-chip, curvilinear ILT mask in 12 hours [20]. The next question is, can the VSB mask writer write curvilinear ILT masks within this same time frame? Figure 10 is a write-time comparison chart between VSB and their multi-beam machine presented by NuFlare [28]. Because VSB mask write time is proportional to the number of shots, according to this NuFlare chart, it is only when shot count is greater than 200 Gshots/pass that VSB write times exceed 12 hours; below the 200 Gshots/pass level, VSB write times are faster than 12 hours even at 75 uC/cm^2. When this number is converted into shot density per square micron, it turns out the magic number is 36 shots/um^2. If the shot density is below this number, the mask write time using a VSB mask writer (i.e., NuFlare EBM 9500) will be less than 12 hours.

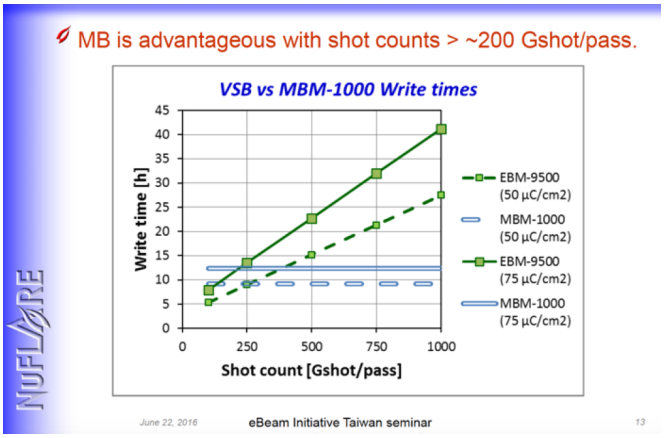
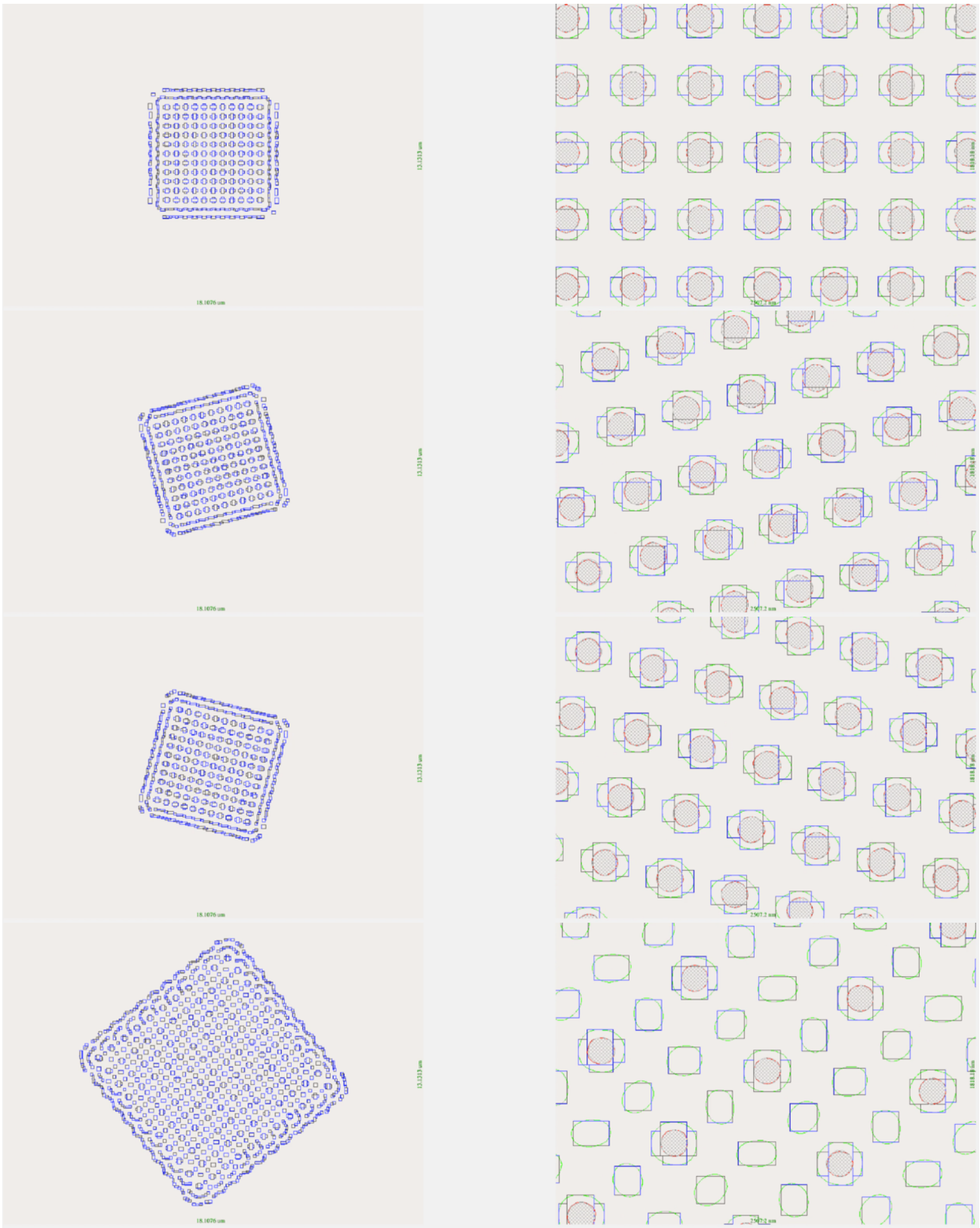


Figure 10: NuFlare's estimation of mask write time for their VSB mask writer and multi-beam mask writer [28]

3.2 Curvilinear ILT Mask Results Using MWCO

This section demonstrates the simulation-based results of MWCO using the same contact array sequence used in the 2019 paper that introduced the new approach to curvilinear ILT [20]. The contact array sequence includes features in dense placement all the way to nearly isolated features, with the contact array rotated to demonstrate the underlying curvilinear, all-angle, nature of this solution. We applied MWCO to each pattern in the sequence to generate an overlapping VSB shot solution for each pattern. Figure 11 shows some examples in this sequence.



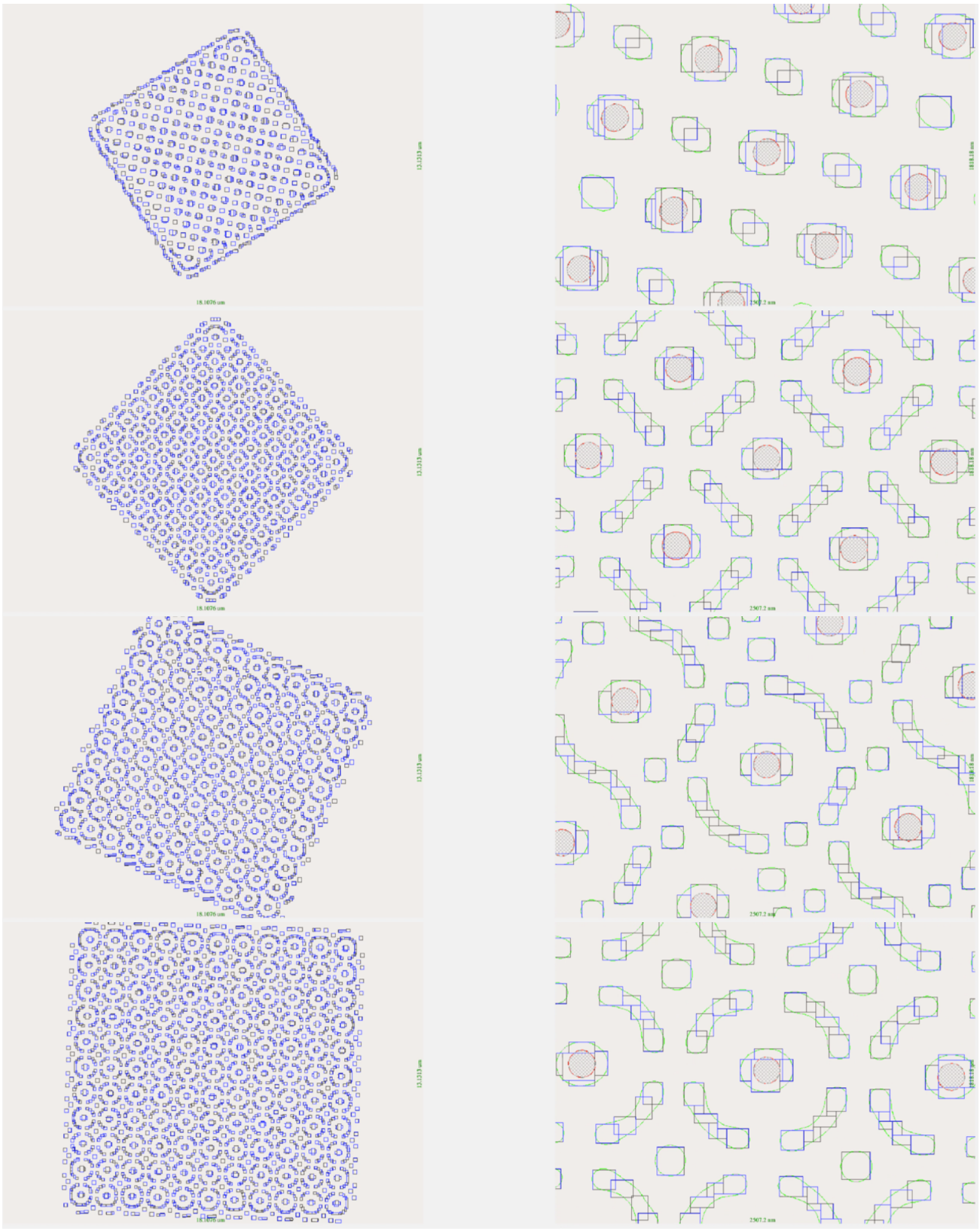


Figure 11: MWCO results for contact array sequence from 2019 paper

VSB shot density for each configuration in this array sequence is computed and shown in Figure 12. Since this array sequence includes different sizes and rotations, effective areas that cover only the actual array region are used in the calculation; in other words, the empty area outside of the array is not used in the calculation, and therefore does not bias the shot density. The chart shows the shot density for every configuration is below 36 shots/um^2. There are three general regions in this sequence. The first region is dominated by main features. In this region, using bigger jogs/shots by using mask-wafer double-simulation is the magic behind the shot-count reduction. The second region is dominated by SRAFs. In this region, using overlapping shots on SRAFs dramatically reduces the shot count to keep shot density below 36 shots/um^2. The third region is still dominated by SRAFs, but due to a larger pitch, the pattern-density is lower, making the shot density even lower than the first or second regions – well below 36 shots/um^2. The chart also shows that using conventional shots (the red line) results in shot densities that are much higher, with minimum about 180 shots/um^2, which translates to about 5X the write time. For the second region, due to curvilinear SRAFs, the write time for conventional shots skyrockets, to 10X.

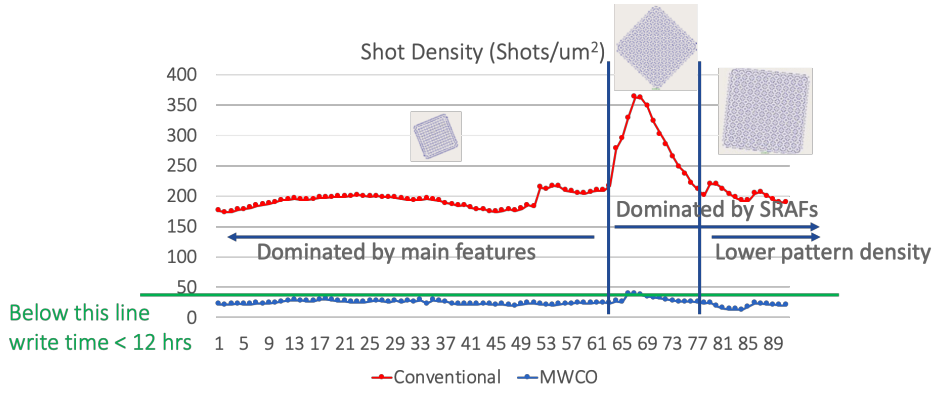
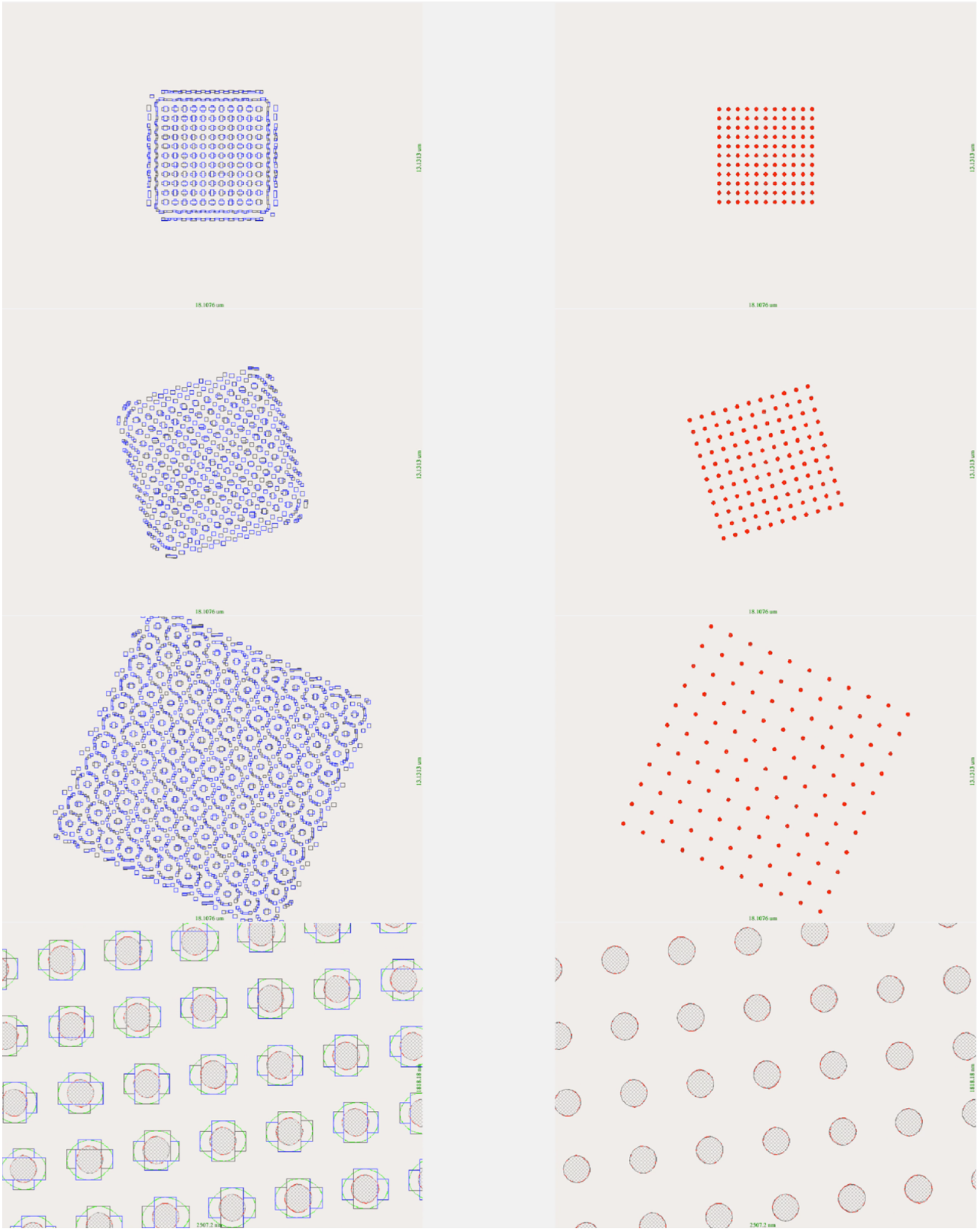


Figure 12: VSB shot density of MWCO results for the contact array sequence from Figure 11

Figure 13 shows VSB shots and simulated wafer contours. The bottom pictures are zoomed in to show that the simulated wafer contours are all very close to the wafer target, meaning the VSB shots resulting from MWCO can print the entire contact array sequence with very high pattern fidelity.



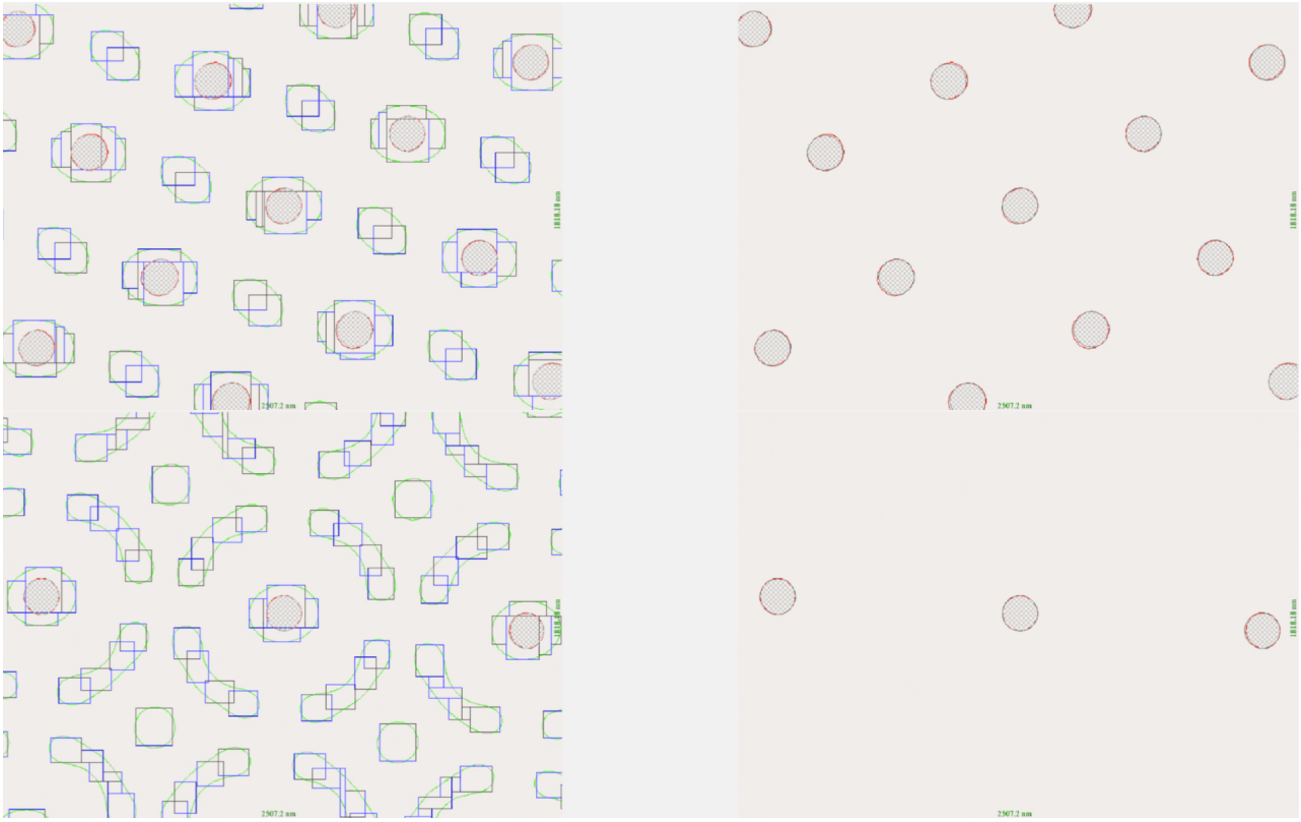


Figure 13: MWCO results for the same contact array in the 2019 paper. In each pair, the ones on the left are MWCO VSB shots of curvilinear mask designs for different pitches and orientations, the ones on the right are corresponding wafer target and simulated wafer contours

4. SUMMARY AND CONCLUSIONS

ILT Vision Realized: Full-Chip Curvilinear ILT in a Day and Full Mask Multi-Beam or VSB Writing in 12 hours for 193i

For more than a decade, the semiconductor industry has recognized the value of ILT in addressing the challenges of advanced-node lithography. Until now, runtime and VSB write-times have been insurmountable barriers to using ILT as a full-chip solution. By embracing a unique, holistically conceived, purpose-built system of GPU-accelerated hardware and software that emulates a single giant GPU/CPU pair, stitchless, curvilinear, full-chip ILT in a day has been demonstrated in the 2019 paper.

This paper introduced Mask-Wafer Co-Optimization (MWCO) as a further enhancement, combining overlapping shots with mask and wafer double-simulation to demonstrate that curvilinear ILT for 193i is practical with VSB mask writers. The results showed that by employing MWCO, VSB writers can write a curvilinear ILT mask with 36 shots/um^2 which for resist sensitivities expected for 193i masks should be below 12 hours in write time.

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