<u>**FOR IMMEDIATE RELEASE**</u>

D2S ENABLES "STITCHLESS" FULL-CHIP INVERSE LITHOGRAPHY TECHNOLOGY IN A SINGLE DAY FOR THE MULTI-BEAM ERA

TrueMask® ILT employs a unique GPU-accelerated approach that emulates a single, giant GPU/CPU pair that can compute an entire full-chip ILT solution at once

SAN JOSE, Calif., September 16, 2019—D2S, a supplier of GPU-accelerated solutions for semiconductor manufacturing, today introduced TrueMask® ILT, a GPU-accelerated hardware and software system that enables IC manufacturers to implement stitchless, full-chip inverse lithography technology (ILT) for advanced-node designs in a single day. TrueMask ILT is a holistically conceived, purpose-built system with every component – including hardware, software, models, visualization and verification – designed and optimized for ILT. This system employs a unique GPU-accelerated approach that emulates a single, giant GPU/CPU pair that can compute an entire full-chip ILT solution at once. The result is a breakthrough in computational performance that finally makes full-chip ILT a practical solution for improved design manufacturability.

Engineers from Micron Technology, a leading memory manufacturer, co-authored a paper with D2S that highlights TrueMask ILT, titled "Study of mask and wafer co-design that utilizes a new extreme single instruction, multiple data (SIMD) approach to computing in memory manufacturing". The paper will be presented orally at the SPIE Photomask Technology 2019 Conference in Monterey, Calif., on Tuesday, September 17 in Session 8 on Mask Data Prep MDP and Curvilinear Data Handling.

"In our joint study with D2S, we examined the benefits of a mask and wafer co-design, which leverages and maximizes GPU acceleration to implement full-chip curvilinear ILT for advanced semiconductor memory manufacturing," stated Ezequiel Russell, Senior Director of Mask Technology at Micron. "The results of this joint study show that curvilinear ILT provides larger process windows compared to conventional ILT or complex OPC."

Full Chip in a Day: The Holy Grail of ILT

ILT is a rigorous computational approach to determine the mask shapes that will produce the desired on-wafer results. Studies have shown that ILT – in particular, unconstrained curvilinear ILT – can produce the best results in terms of resilience to manufacturing variation. Until recently, two major obstacles have kept ILT from being widely applied. One of these barriers – the ability to write curvilinear mask patterns – was eliminated recently through the introduction of multi-beam mask writers, which can write any shape without a time penalty. The second barrier – long runtimes due to the sheer volume of computations required to perform full-chip ILT – has remained unresolved until now.

Previous attempts to overcome this final hurdle involved dividing the chip into partitions, running the computations for each partition in parallel, and then "stitching" the partitions back together. However, chip partitioning introduces errors that must be corrected once the partitions are stitched together. This correction, in turn, requires additional computations, which can give rise to additional stitching errors. A "stitchless" solution avoids both the runtime increase and stitching artifacts.

"For years, ILT has been seen as a promising solution to many of the challenges of advanced-node lithography, but the ability to implement ILT across the entire chip layout in a timely fashion had been out of reach," according to Dr. Leo Pang, chief product officer and executive vice president at D2S. "Wafer fabs need to deliver wafers in the shortest time possible, which requires ILT process time to be shrunk to a single day in order to be practical. D2S TrueMask ILT is the first commercial ILT solution that delivers full-chip ILT within this time constraint."

A Purpose-Built System Enables Stitchless, Full-Chip ILT In a Day

The rise of GPU-accelerated computing for scientific applications has offered a new opportunity to bring a practical full-chip ILT solution to market. However, simply using GPU-accelerated computing to speed the computations of individual chip partitions has proven unsuccessful because stitching errors continued to erode the runtime gains afforded by GPU acceleration. D2S reasoned that what was needed was the ability to process the entire chip at once. By taking a "from the ground up" holistic approach, D2S was able to build an ILT-specific computing appliance designed to emulate a giant GPU/CPU pair that optimizes full-chip data seamlessly.

Every component of TrueMask ILT – the GPU-accelerated D2S Computational Design Platform (CDP), curvilinear mask and wafer lithography simulation and verification software, models, geometry libraries, visualization, etc. – was purpose-built for GPU-acceleration and for full-chip ILT computation. Every aspect of the physics and chemistry of wafer lithography and processing has been modeled and optimized synergistically throughout the system in order to reap the largest potential run-time benefits without compromising computational accuracy.

TrueMask ILT Facilitates Curvilinear Shapes for Greater Design Manufacturability

ILT is a mathematical approach that naturally produces curvilinear shapes. Curvilinear mask shapes are more resilient to manufacturing variation. With multi-beam mask writing now available, curvilinear shapes no longer require additional time to write. TrueMask ILT was built to leverage the power of multi-beam mask writing and is optimized for curvilinear mask output, which is critical for advanced designs manufactured with both optical and EUV lithography.

A backgrounder detailing the importance of stitchless, full-chip ILT in a day can be downloaded at https://design2silicon.com/products/truemask-ilt. Videos featuring D2S spokespeople describing TrueMask ILT will be available soon and can also be viewed here.

About D2S
D2S is a supplier of GPU-accelerated solutions for semiconductor manufacturing. The company provides simulation-based custom solutions to leading equipment partners. D2S TrueMask® solutions use the D2S Computational Design Platform to enable advanced photomask designs using complex shapes for superior wafer quality within practical, cost-effective write-times. D2S is the managing sponsor of the eBeam Initiative and a founding member of the Center for Deep Learning in Electronics Manufacturing (CDLe). Headquartered in San Jose, Calif., the company was founded in 2007. For more information, see: www.design2silicon.com.

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Contact:
David Moreno
Principal
Open Sky Communications
Tel: +1.415.519.3915
E-mail: dmoreno@openskypr.com

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