Agency Contact:
David Moreno
MCA
Tel: +1-650-968-8900, ext. 125
E-mail: dmoreno@mcapr.com

D2S UNVEILS INDUSTRY'S FIRST MASK-WAFER DOUBLE SIMULATION PLATFORM

TrueMask™ DS enables interactive optimization of mask write-times and wafer quality

SAN JOSE, Calif., September 20, 2011—D2S™, a supplier of computational design platforms, today introduced TrueMask™ DS, the industry's first mask-wafer double simulation accelerated workstation for R&D exploration, bit-cell design, hot-spot analysis and mask-defect categorization that comprehends overlapping eBeam shots and dose modulation. TrueMask DS is an essential tool for mask shops and wafer fabs in qualifying and optimizing 20-nm-node and below designs, where assist features on photomasks that are smaller than 80 nm in size can no longer be produced faithfully and have an increasing impact on wafer yields.

"Mask features at below 80 nm occur frequently at 20-nm logic nodes and below. Increasingly sophisticated technologies are required to print these features accurately on mask," stated Naoya Hayashi, research fellow, Dai Nippon Printing Co. (DNP). "Of particular interest are sub-resolution assist features (SRAFs) and other small features that decorate the mask to improve wafer quality. Particularly for critical circuits, mask customers are interested in making a balanced trade-off between wafer quality achievable with complex optical proximity correction (OPC)/inverse lithography technology/source mask optimization and the cost and turnaround time of masks. An interactive mask-wafer double simulation would enable efficient exploration of these trade-offs for critical circuits."

OPC has been used for years to add SRAFs on photomasks to compensate for the optical effects of sub-wavelength lithography that prevent small features from printing correctly. At the 20-nm node and beyond, the shapes of these SRAFs as well as main features must become more complex to produce the desired images with sufficient process window on the wafer. This added data causes mask write-times to skyrocket—requiring necessary engineering trade-offs between acceptable wafer accuracy and tolerable mask-write times.

-more-

In addition, as these assist features shrink to below 80 nm in size, there is no longer a guarantee that they can be reproduced as desired on the photomask due to the combination of short-range blur of the electron beam used to write the masks and the effects from the mask develop, bake and etch processes. In other words, the very features needed to ensure accurate patterning are now printing inaccurately themselves.

"Lithography simulation is no longer enough to validate mask designs for leading-edge devices," stated Aki Fujimura, CEO of D2S, the managing company sponsor of the eBeam Initiative. "Implementing mask-wafer double simulation is absolutely necessary in order to have a clear understanding of how mask shapes will be produced on both the mask and the wafer plane. TrueMask DS is a valuable tool through many phases of design to manufacturing, including for mask engineers, product engineers, OPC engineers, memory-cell designers and test-chip engineers."

Deploying hardware acceleration, TrueMask DS can produce a double simulation of the mask and wafer for 5x5 micron (on wafer) areas at interactive speeds. Users can experiment using different variable-shaped beam (VSB) shots to write the masks, as well as using overlapping shots and dose modulation—techniques that can be employed to reduce mask write times and improve CD uniformity, respectively. Then, users can instantly see the contour shape of the exposed resist, and within seconds see an overlay of the lithography aerial image that would be printed on the wafer.

TrueMask DS features include:

- 0.1-nm-resolution mask simulation up to 300x300 micron (mask dimensions), including overlapping shots and dose modulation
- Advanced eBeam modeling with arbitrary point spread functions for exploration
- Fast, interactive aerial litho simulation from hardware acceleration
- 5x5 micron (on wafer) interactive mask-wafer double simulation
- SEM interface for overlay analysis of pictures with simulations

TrueMask DS is available today. For more information on TrueMask DS, visit www.design2silicon.com/products_TrueMask_DS.

About D2S, Inc.

D2S is a supplier of computational design platform to maximize existing eBeam technology to reduce mask costs for both low- and high-volume applications. D2S advanced design-for-eBeam (DFeB) mask solution reduces mask write times for high-volume designs with complex and circular features using existing eBeam mask writing equipment. D2S DFeB direct write solution virtually eliminates the costs of masks for low-volume applications and can speed time-to-market by shortening the design-to-lithography process flow. D2S is the managing sponsor of the eBeam Initiative. Headquartered in San Jose, Calif., the company was founded in 2007. For more information, see: www.design2silicon.com.

###