

D2S

D2S (Direct2silicon) was founded in 2007 to provide software and IP that

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enables direct write e-beam lithography, making low-volume silicon production cost effective at the 65-nm node and below. D2S recently closed more than \$9 million in Series B financing in an up-round led by Benchmark Capital and DAG Ventures, with all prior Series A investors, including Advantest and Cadence, participating.

As the industry moves to smaller geometries, mask costs become an even bigger challenge for IC manufacturers, making low-volume production of custom ICs economically infeasible. With mask budgets above \$3 million at 40-nm, even derivative designs that have relatively low design costs cannot be produced without a large upfront volume commitment.

D2S' design-for-e-beam (DFEB) technology enables SoCs to be manufactured without the upfront mask cost. For modest production runs of 100,000 chips or less, direct write techniques are more cost effective by eliminating mask costs. The D2S technology has been in development since 2002.

DFEB is a design-to-manufacturing approach to enhance the throughput of e-beam (EB) lithographic exposure. DFEB uses character or cell projection (CP) technology combined with

design and software techniques to reduce a design's required shot count, resulting in increased CP e-beam direct-write (EbDW) throughput. Depending on the layer and design, D2S can improve the Character Projection (CP) based e-beam direct write by 10-25X in e-beam shot count.

Without the need to rely on a lithography shift, DFEB maximizes and enhances current e-beam technology. By efficiently employing the e-beam direct-write (EbDW) approach, DFEB eliminates the cost of masks and can speed time-to-market by shortening the design-to-lithography process flow.

Early market development is already underway with global industry leaders. In February 2009, D2S launched the eBeam Initiative (www.ebeam.org) with a group of 19 other companies throughout the entire semiconductor ecosystem to promote DFEB technology. Charter members include: Advantest, Alchip, Altos Design Automation, Cadence, CEA/Leti, D2S, Dai Nippon Printing, e-Shuttle, eSilicon, Fastrack Design, Fujitsu Micro, Magma, Tela Innovations, Toppan Printing, Virage Logic and Vistec Electron Beam Lithography Group.

The eBeam Initiative aims to increase investment in multiple supply chains and reduce the barriers to adoption, leading to an accelerated implementa-

tion among a broad number of customers. The formal steering group consists of Advantest, CEA/Leti, D2S, e-Shuttle, Fujitsu Microelectronics and Vistec, with D2S serving as the managing sponsor. Various eBeam Initiative members have already collaborated to validate maskless manufacturing with successful test wafers for the 45-nm and 32-nm nodes.

D2S estimates the market size at \$300M. D2S believes that all prototypes and engineering samples should eventually be built maskless, as there is no point in paying for masks when there is no certainty of a volume business. Assuming a \$20M machine that takes one day to write all layers by e-beam, the cost of lithography per wafer is \$20K. If the total mask budget (which typically takes multiple mask sets) is \$2M at 40nm, the break-even is 100 wafers or less.

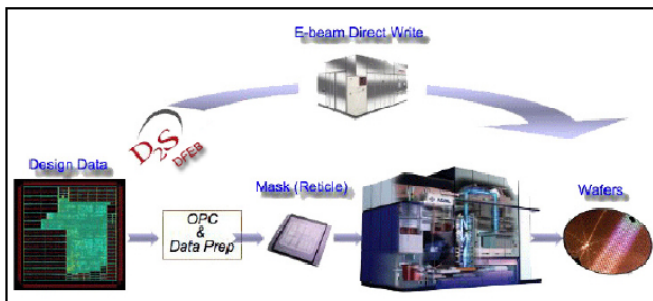
Furthermore, the company believes that the majority of high value, lower-volume derivative chips should also be built maskless. More than half of ASIC/ASSP tape-outs end up having fewer than 100 wafers production. All of these designs should be maskless as well.

D2S has collaborations with Fujitsu-e-Shuttle, and with research fab Vistec-CEA/Leti. D2S's goal is to have multiple sources of maskless SOCs by 2011. A product announcement is anticipated later this year.

Aki Fujimura, Chairman and CEO (previously CTO at Cadence, President/COO of

Simplex Solutions, VP at Pure Software, and a founding member of Tangent Systems)

James Fong, Ph.D, Chief of Staff and Interim CFO (previously Director of Engineering with Cadence and



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Director of Central Engineering at Simplex Solutions)

Kenji Yoshida, Ph.D, President and Representative Director of D2S KK, Japan (previously CTO of Cadence, Japan and Fellow and GM of Design Technology at Semiconductor Academic Research Center in Japan)

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Cliff Rants

D2S – Direct Write E-beam Lithography Acceleration Software

For modest production runs, direct write techniques would seem to make sense –right? That's D2S' premise. D2S focuses on accelerating e-beam direct-write (EbDW) throughput via a variety of techniques. This approach could be a boom for the prototype, university/govt. and small production run market, enabling previously cost-prohibitive undertakings. I think this approach makes a lot of sense. The only monkey wrench? At what point does it make sense to simply use merchant FPGAs, which are rapidly becoming the prototype and even low-volume production vehicle of choice.

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